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DIGITAL FEEDBACK SEISMOMETER STUDY

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Several methods are examined for obtaining digitized output data from the Geotech 36000 horizontal sensing seismometer in borehole installations. Configurations using either ternary or binary pulse width modulated torque-to-balance loops were found to be unsatisfactory. Analog-to-digital conversion of the output signal down-hole was found to be acceptable and a system using a digitizer within the seismometer feedback loop is recommended.

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SUMMARY

The following analytical study examines the application of digital technology to seismometer measurements in borehole installations. Current practice is to generate within the seismometer system an analog output proportional to seismic input and transmit this signal in analog form to the top of the borehole. The inherent disadvantages of transmitting low level analog signals over long transmission lines underline the importance of converting the signal output to digital form at the bottom of the borehole.

Several methods of digitizing the seismometer output were examined. Two methods involved closing a digital torque-to-balance loop around the seismometer. Both ternary (three state) and binary (two state) loop implementations were analyzed and simulated using an IBM-360 computer. The ternary loop was found unacceptable since it resulted in the generation of an input dependent noise signal riding on the desired output. This noise could not be filtered since it could vary over a wide frequency band.

The binary pulse width modulated loop performed well in the computer simulation. However, use of the binary loop resulted in the generation of a high ripple signal summed with the desired error signal. The presence of this signal put impractical requirements on the electronics within the control loop, thus eliminating the binary loop from further consideration.

The two remaining implementations studied involved the use of an analog restoring loop in conjunction with an analog-to-digital (A/D) converter. The A/D converter was assumed to be either inside the control loop or external to the loop. The configuration with the A/D conversion inside of the loop proved far superior and resulted in an overall system performance which was quite good.

The worst case noise caused by the A/D converter was only slightly higher than the noise in the current analog loop configurations (11 μV rms (0-10 Hz) vs 4 μV rms (.02-1 Hz)).

The A/D converter provides an 18 bit dynamic range and retains the simplicity of the add-on external approach. The electronics design, discussed in detail in Chapter 5, can be built at reasonable cost and requires no overly complex circuitry. Errors due to nonlinearities, temperature variations and other instabilities would be reduced by the loop gain and could be made negligible. In the case of the outboard A/D converter there would be no reduction of these errors and additional effort

would be required to adequately compensate for them.

The study concludes that the inboard A/D converter provides an attractive alternative and recommends that an 18 bit A/D converter be interfaced with a Geotech 36000 instrument and the resultant performance be evaluated at a "seismically quiet" site.

CHAPTER 1

INTRODUCTION

In recent years the development of sophisticated digital control and encoding techniques has made available to related disciplines the numerous advantages inherent in such techniques. At Draper Laboratory digital control loops have been put to large scale use with a variety of inertial grade instruments. For example, a ternary force-rebalance loop is used in the Poseidon guidance system with the Draper Laboratory size 16 PM PIP. The loop provides quantized increments of velocity data. Similar work using binary and pulse width modulated control loops with gyros and accelerometers has been done in hardware design optimization studies. The effort in these areas has been to achieve a high level of resolution with extremely good long-term pulse weight stability.

The work described in the present report is an attempt to apply digital technology to seismometer systems. The candidate instrument used in the analysis was the Geotech 36000 horizontal sensing seismometer. This instrument was modelled with both ternary and binary pulse width modulated control loops. In addition, an analog configuration was evaluated employing either inboard (within the feedback loop) or outboard A/D conversion of the analog output. Computer simulations were used to verify linearity and loop stability and to examine the loop response to simulated inputs.

Chapter 2 contains a brief description of the Geotech 36000 instrument. A basic analytical model is derived and a brief summary of instrument operating specifications is presented.

Chapter 3 presents a theoretical analysis of the various digital implementations used with the basic seismometer model. Most of the chapter is devoted to a detailed design of the pulse width modulated binary configuration, since this configuration appeared to be the only viable fully digital implementation. A prime disadvantage of this configuration is the large ripple component riding on the desired dc error signal. This ripple was not at first considered to be a serious problem; however, when the electronics design was done in detail (as shown in Chapter 5) it was discovered that the presence of the large ripple component necessitates use of a sample and hold circuit with an accompanying large phase lag. The total loop configuration becomes unstable and extremely difficult to implement, if at all possible.

The latter portions of Chapter 3 examine an analog configuration with A/D

conversion within the control loop. Though this approach was the last chosen for analysis, it exhibits definite advantages over the other approaches and an attractive option for further development.

Chapter 4 details a basic approach to the electronics design taking into account the seismometer design goals, while attempting to maintain a final design concept which remains both feasible and economical. The detailed electronics design is presented in Chapter 5. The approach taken is general in form, applying in varying degrees to all of the digital implementations described in Chapter 3. The result of the study is the highlighting of some of the problems associated with the various implementations and a selection of the inboard A/D conversion as that approach appearing to offer the most promise. An analysis of the noise resulting from the A/D converter is presented in Chapter 6.

Chapter 7 presents conclusions resulting from the study and recommendations for future effort.

CHAPTER 2

DESCRIPTION OF THE 36000 SEISMOMETER OPERATION

2.1 Physical Description and Operation

The 36000 seismometer is a horizontal sensing pendulous type device capable of measuring long period seismic disturbances (periods of 10 to 100 seconds). The seismometer assembly consists basically of a mechanical spring restrained pendulous mass attached to the case or frame of the seismometer and free to pivot in a single plane. Provisions are available for both dissipative damping (internal friction and external electronics) and nondissipative damping. In addition, an electrodynamic transducer (moving coil) is used for electronic feedback spring control.

Motion of the pendulum or mass with respect to the case is measured by a displacement transducer consisting of a capacitance bridge arranged such that the capacitance varies linearly with motion of the mass. The bridge is excited by a carrier signal of constant magnitude and frequency. Movement of the pendulum is, therefore, translated into an amplitude modulated signal. A photograph of the 36000 assembly is shown in Figure 2.1-1.

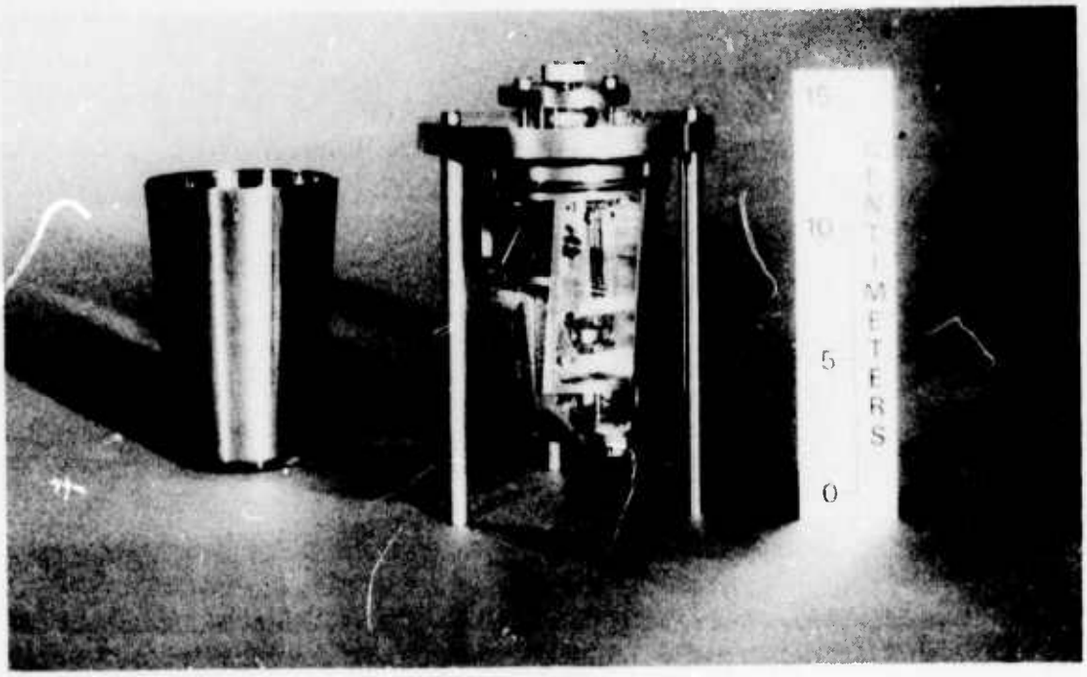

Fig. 2.1-1 Geotech 36000 Seismometer

A block diagram of the system is depicted in Fig. 2.1-2. The carrier signal is amplified by an IF amplifier and then demodulated to yield an analog signal. This signal is measured and fed back to the electrodynamic force generator to provide restraint on the motion of the pendulous mass. Additional electronics divide the signal into low and high frequency intervals (less than and greater than 0.02 Hz) and provide necessary loop compensation.

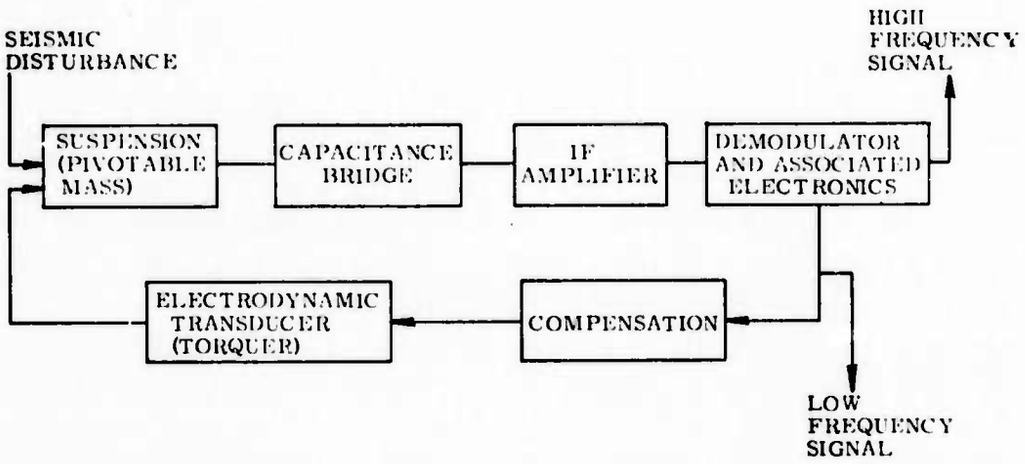

Fig. 2.1-2 Basic Block Diagram of Seismometer

2.2 Modeling of the Seismometer

The suspension block depicted in Fig. 2.1-2 was modelled as a garden gate type of device sensing accelerations in the horizontal plane with the axis of the pivot vertically oriented (see Figure 2.2-1).

Let:

- M = mass of the boom (kg)
- k = radius of gyration (m)
- θ = angular displacement of the mass (rad)
- d = damping constant (N-m-s/rad)
- K = spring constant (N-m/rad)
- r = pivot-center of gravity separation (m)
- x = horizontal acceleration of the case (m/s^2)

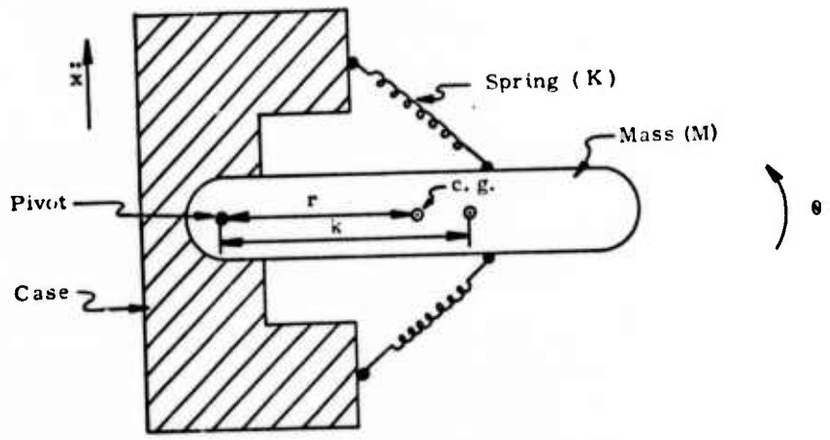

Fig. 2.2-1 Garden Gate Suspension Block

Summing of the torques about the pivot yields:

$$Mk^2\ddot{\theta} + d\dot{\theta} + K\theta - Mr\ddot{x} = 0 \qquad (2\text{-}1)$$

Taking LaPlace transforms of both sides, the transfer function relating angular displacement to input acceleration is obtained.

$$\frac{\theta(s)}{\ddot{x}(s)} = \frac{Mr/K}{Mk^2s^2/K + ds/K + 1} \qquad (2\text{-}2)$$

The capacitance bridge, IF amplifier, demodulator and other amplification were modelled as C_0K_0.

Dynamics of the associated electronics which divide the analog signal into low and high frequency bands yield the following transfer function:

$$(T_1s/(1 + K_o) + 1)/(T_1s + 1) \qquad (2\text{-}3)$$

where $T_1/1+K_0$ corresponds to 50 seconds and T_1 to 10,000 seconds.

The compensation block provides lead phase to compensate for the lag phase introduced by the suspension and the signal divider. A resistor and capacitor in parallel give the requisite lead for the loop and current levels for the torquer. The transfer function relating current to voltage is given by:

$$i(s)/e(s) = (T_2 s + 1)/R \qquad (2\text{-}4)$$

where:

R = resistance

and T_2 corresponds to about 1.8 seconds and compensates for the 180° phase shift introduced by the suspension at its natural frequency of 5 seconds.

Finally, the torquer is represented as a simple gain with the units of $m/s^2/A$.

This linear model of a seismometer loop provides the point of departure for the analysis of other configurations discussed in Chapter 3.

2.3 Noise Specification and Instrument Parameters

The design of a good seismometer requires that the earth motion equivalent of thermal agitation noise introduced by the suspension and the associated electronics should be 20 db below seismic background noise.

At a quiet deep mine, such as that located at Queen Creek, Arizona, the minimum background noise level (at 0.035 Hz) is 3.4×10^{-10} $m/s^2/\sqrt{Hz}$. The maximum noise level introduced by the seismometer should be 20 dB down from this value or 3.4×10^{-11} $m/s^2/\sqrt{Hz}$. This is considered to be a design optimum.

Table 2.3-I presents a tabulation of parameters and specifications for the 36000 instrument. The noise level of the Geotech instrument equals 4×10^{-11} m/s^2 (0.02 to 1 Hz).

The maximum long period output signal level stated in the Geotech specification (0.02 to 1 Hz) corresponds to 10^{-4} m/s^2 input to the seismometer. If the minimum signal to be detected is at the noise level of the instrument, then a dynamic range of 2×10^6 is required. This value is equivalent to a 21 bit digitization. The specifications further call for 10% linearity over the dynamic range.

Table 2.3-I

Parameters and Specifications for the 36000 Seismometer

Parameters

Inertial Mass	0.364 kg
Radius to Center of Mass	0.0432 m
Spring Constant	1.0×10^{-3} N-m/rad
Moment of Inertia	6.33×10^{-4} kg-m^2
Dissipative Damping	1.17×10^{-5} N-m-s/rad

Specifications

Input

Equivalent Noise (0.01 to 1 Hz)	1.56×10^{-21} $(m/s^2)^2$/Hz, max.
Maximum Input Levels	$\pm 1 \times 10^{-2}$ m/s^2

Output

Noise Level (0.02 to 1 Hz)	1.6×10^{-11} V^2/Hz, max.
Sensitivity	1×10^5 V/m/s^2 ±5%
Offset	±5V, max.
Maximum Level	±10V
Response	Flat to acceleration input from 0 to 1 Hz, down 12 dB/octave above 1 Hz.

CHAPTER 3

ANALYSIS OF FOUR DIGITAL SEISMOMETER CONFIGURATIONS

3.1 Introduction

Four digital seismometer configurations were analyzed with respect to their ability to produce a linear response in an environment of accelerations ranging from 10^{-10} to 10^{-2} m/s^2 with periods of 15 to 45 seconds. It should be noted that the total dynamic range of the Geotech feedback loop is 10^8. Each of the outputs in the current Geotech configuration (0-1 Hz; 0.02-1 Hz) has a dynamic range of 10^6. The initial study presented here examines a pulse torque feedback implementation giving a 10^6 dynamic range while utilizing the output voltage range employed by Geotech.

The point of departure for the overall analysis of digitized seismometer systems was the analog configuration presently used by Geotech. Necessary modifications were made to this configuration to achieve the required digital performance.

The linear configuration for an analog accelerometer system was derived in Chapter 2 and is shown as the block diagram in Fig. 3.1-1.

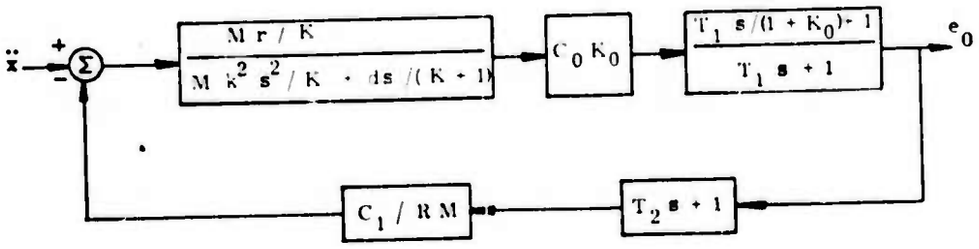

Fig. 3.1-1 Linear Model of Analog Seismometer System

where the variables are again defined as in Chapter 2, with the addition of:

C_0 = AC amplifier gain (V/rad)
K_0 = DC amplifier gain (V/V)
T_1 = time constant associated with DC amplifier (seconds)

s = LaPlace transform operator

T_2 = time constant associated with stabilization (seconds)

C_1 = torquer constant (N/A)

R = resistance (V/A)

The system of Fig. 3.1-1 generates continuous information relating to acceleration. Four alternatives which provided a digitized measure of the displacement x were studied.

3.2 Ternary System

The ternary system is essentially a rate measuring device. Signal derivative information is converted to a pulse rate. The pulses activate the torquer of the seismometer and a count of the pulses yields velocity information. Figure 3.2-1 shows the operation of a typical ternary system.

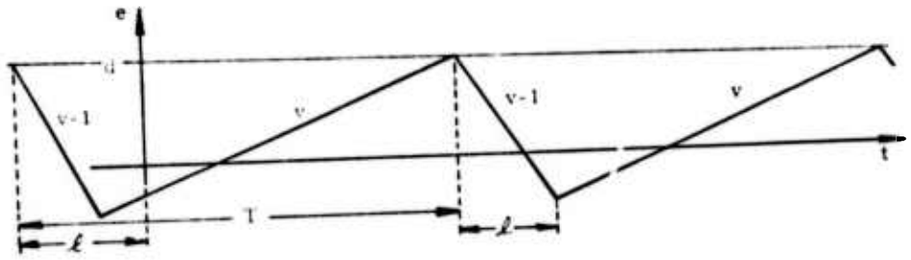

Fig. 3.2-1 Steady State Ternary Operation

The following discussion pertains to signals of positive slope. A simple extension may be made to signals of negative slope.

Let e be a signal with positive slope v. Let d be a threshold activating voltage. When the signal level e reaches d, a pulse of amplitude -1 is subtracted from slope v for a time interval ℓ. The system then resumes "pulseless" operation until the next threshold is reached. This operation is shown in Fig. 3.2-2. Dotted lines imply logical connectors.

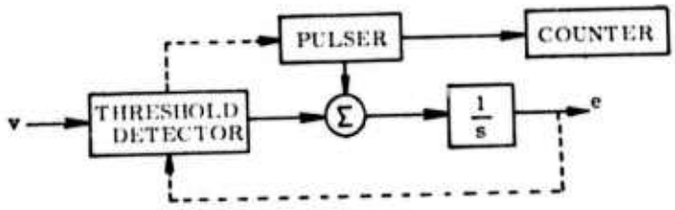

Fig. 3.2-2 Block Diagram of Ternary Configuration

To determine the relationship between pulse counts and v assume steady state (constant v). Let T be the time between the beginning of the last pulse and the time that threshold d is reached.

For steady state, an examination of Fig. 3.2-1 shows that:

$$v(T - \ell) = -(v - 1)\ell \quad \text{or} \quad v = \ell/T \tag{3-1}$$

i.e., the time between pulses is inversely proportional to v. As the pulse frequency f is equal to 1/T,

$$f = v/\ell \tag{3-2}$$

A counting of the pulses, therefore, yields velocity information.

A major drawback to ternary implementation may be inferred from Eq. 3-2. The frequency of pulses exciting the torquer is a function of the slope of the signal. As the mass responds essentially to the dc value of the pulse train, the pulse train less the dc value is noise corrupting the performance of the system. This noise can not be simply filtered as its frequency is derivative dependent.

As an example, assume that v is required to a resolution of 1 part in 250,000. To avoid noise frequencies near the natural frequency of the mass (approximately 5 seconds), T should be less than one second. This in turn places a constraint on the pulse width, ℓ to be less than 4 μs. The noise frequency would then range over frequencies from 1 Hz to 250,000 Hz as a function of the magnitude of v.

3.3 Binary System

The binary system consists of a scheme whereby the torquer of the accelerometer is excited by alternating pulses of fixed magnitude with the constraint that the sum of the periods of the negative pulse (T_0) and the following positive pulse be a constant, T (see Fig. 3.3-1).

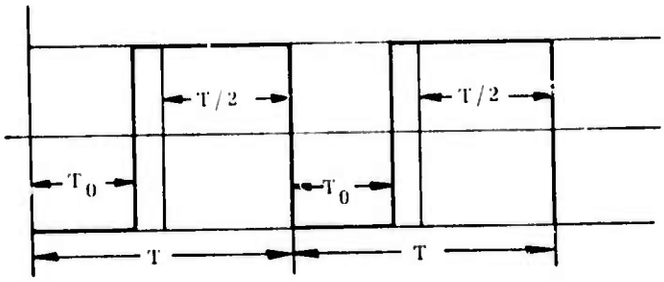

Fig. 3.3-1 Binary System Pulse Pattern

The dc feedback signal to the torquer is then proportional to $\frac{T}{2} - T_0$. Linearity is maintained by making $\frac{T}{2} - T_0$ proportional to some activating voltage. A system incorporating binary feedback is shown in Fig. 3.3-2.

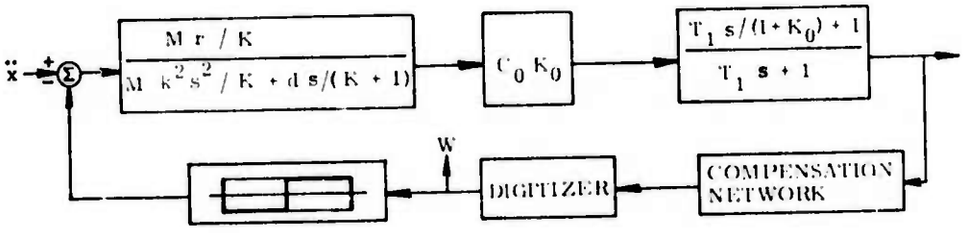

Fig. 3.3-2 Block Diagram for a Binary Seismometer System

A compensation network considerably more complicated than that of the linear system is required because of the delay inherent in the binary implementation. In order to effect full range operation (i.e. a positive pulse lasting for a period T), it is necessary to determine T_0 at the start of a period. The fact that in general the response to a measurement at the start of an interval does not occur immediately constitutes system delay time. System instability will occur if the effect of this delay is not counteracted.

The wave form shown in Fig. 4 may be decomposed into the sum of a square wave and a pulse train (see Figs. 3.3-2a and 3.3-3b).

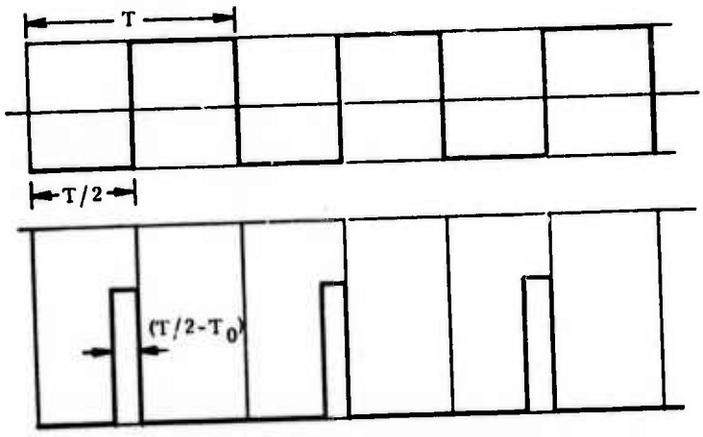

Fig. 3.3-3 Equivalent Representation for a Binary Pulse Pattern

The dc value of the wave in Fig. 3.3-3b constitutes the essential signal feedback.

Let $\Delta T = \frac{T}{2} - T_0$. The digitizer converts the analog signal w to ΔT by the following relationship.

$$\Delta T = -MIN(|w|/w_{max}, 1)SIGN(w)\ T/2 \qquad (3\text{-}3)$$

where w_{MAX} is the analog signal corresponding to full level operation (i.e. $\Delta T = T/2$).

If the maximum acceleration is A_{MAX} and the torquer constant is C_v (N/V), then:

$$w_{max} = A_{max} M/C_v \qquad (3\text{-}4)$$

where M has been previously defined as pendulous mass.

The wave forms of Figs. 3.3-3a and 3.3-3b can be expanded in a Fourier series of period T.

The square wave is given by:

$$-4/\pi \sum_{n_{odd}}^{\infty} \sin(2n\pi t/T)/n \tag{3-5}$$

The pulse train of width, T, is given by:

$$2\Delta T/T - \left[2/\pi \sum_{n=1}^{\infty} (-1)^{n+1} \sin(2n\pi\Delta T/T)\cos(2n\pi t/T)/n\right] \tag{3-6}$$

The total signal driving the torquer is then:

$$\begin{aligned} 2\Delta T/T - P(T) = {} & 2\Delta T/T - 4/\pi \sum_{n_{odd}}^{\infty} \sin(2n\pi t/T)/n \\ & - 2/\pi \sum_{n=1}^{\infty} (-1)^{n+1} \sin(2n\pi\Delta T/T)\cos(2n\pi t/T)/n \end{aligned} \tag{3-7}$$

As the dc term, $\frac{2\Delta T}{T}$, is proportional to w (see Eq. 3-3), the periodic functions of T constitute system noise of known period.

With no input (x = 0) the signal seen by the digitizer is the signal of Eq. 3-7 modified by its propagation through the dynamics introduced by the accelerometer, amplifier, compensation, etc. The steady state w at any sampling time, NT, is given by:

$$\begin{aligned} w(NT) = {} & \left[2\Delta T/T - \left\{2/\pi \sum_{n=1}^{\infty} (-1)^{n+1} \sin(2n\pi\Delta T/T)\right.\right. \\ & \left.\left. \cos(\phi_n)/nG(n\omega_o) + 4/\pi \sum_{n_{odd}}^{\infty} \sin(\phi_n)/nG(n\omega_o)\right\}\right]A \\ = {} & [2\Delta T/T - P]A \end{aligned} \tag{3-8}$$

where:

$A = (Mr/K)C_0K_0A_{MAX}$

$\omega_0 = 2\pi/T$

ϕ_n = phase shift for the n^{th} harmonic

$G(n\omega_0)$ = attenuation of the n^{th} harmonic

P = Value of periodic terms at sampling time

Substituting for ΔT from Eqs. 3-3 and 3-7 yields:

$$w(NT) = -AP/(1 + AC_v/(A_{max}M)$$

$$= \frac{MrC_oK_oA_{max}P/K}{1 + (rC_oK_oC_v)/K}$$

$$\simeq MA_{max}P/C_v \qquad (3\text{-}9)$$

The dc value of wave form, w, is:

$$2A\Delta T/T = w(NT)\,A/w_{MAX} \simeq A\,P$$

$$= rC_oK_oMA_{max}P/(C_vK) \qquad (3\text{-}10)$$

Figure 3.3-4 shows a typical wave form, w, for zero input to the accelerometer.

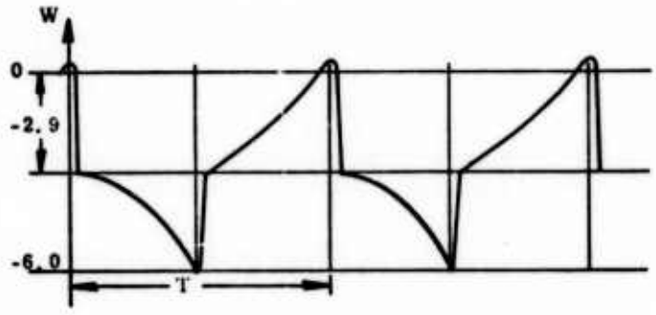

Fig. 3.3-4 Digitizer Input Waveform

Note that from Eqs. 3-9 and 3-10 the ratio of w(NT), the sampled signal, to the dc value (essentially the maximum amplitude of the periodic wave) is:

$$rC_oK_o/K$$

This quantity will be discussed later in the evaluations of the four digital implementations.

The compensation network shown in Fig. 3.2-2 has the following transfer function:

$$\frac{[T_2^2 s^2 + aT_2 s + 1][T_4^2 s^2 + cT_4 s + 1]}{[T_3^2 s^2 + bT_3 s + 1]}$$

The sampling technique (measuring at NT and responding at $(N + \frac{1}{2})$ T) introduces a phase lag equal to the following:

$$\pi(\omega/\omega_o)$$

where ω is the frequency of the signal being measured. As the mass introduces 180^o of lag shortly after its 5 second breakperiod, it is necessary to compensate for this delay to prevent instability.

The lead network chosen is:

$$T_4^2 s^2 + cT_4 s + 1$$

where:

$T_4 = T/\pi$
$c = \pi/1.8$

This network compensates for the phase lag introduced by periods greater than 0.2 second.

The remainder of the compensation,

$$\frac{[T_2^2 s^2 + aT_2 s + 1]}{[T_3^2 s^2 + bT_3 s + 1]}$$

where:

$T_2 = 6/2\pi$, $a = 0.2$
$T_3 = 12/2\pi$, $b = 2.0$

was introduced to attenuate high frequencies ($>2\pi/T$), thus allowing an increase in loop gain.

A plot of magnitude and phase vs frequency for open loop and closed loop response is shown in Figs. 3.3-5a, b, c and d. Linearity was found to extend over signal levels ranging from 10^{-3} m/s^2 to 10^{-8} m/s^2 to four places. Between 10^{-3} and 5×10^{-3} accuracy tapered off to two places (see Fig. 3.3-6).

Amplitude was determined to be independent of period for input in the 20 to 40 second range (see Figs. 3.3-7, 3.3-8 and 3.3-9).

Figure 3.3-10 shows the effect of starting out in saturation. An eight second recovery period is indicated.

The high frequency oscillation (ringing) occurring during the first eight seconds in Figs. 3.3-7 through 3.3-10 is caused by the transient effect of starting the system. The frequency of ringing corresponds to the frequency at the -180° ordinate in Fig. 3.3-5d.

An evaluation of the binary system points up two basic weaknesses. The first which is encountered in all sampled-data systems is aliasing. Aliasing occurs when the signal being sampled contains frequency components greater than 1/2 the sampling rate. This condition is tolerable if only a small portion of information lies in the proscribed frequency range.

The second drawback is due to the relatively high level of noise in the form of periodic functions existing at the digitizer. It was mentioned earlier that the ratio of the amplitude of the periodic signal to signal for no input is rC_0K_0/K. For the parameters considered in the present application, $rC_0K_0/K \approx 10^8$. Due to the delay inherent in the operation of the system, essentially no filtering can be performed on the fundamental of the periodic functions as attenuation introduces intolerable phase lag (instability). Although, theoretically, the size of this "noise" creates no problem in determining the signal, hardware considerations preclude the accurate measurement of the signal in the presence of the large, rapidly changing, periodic function (see Chapter 5).

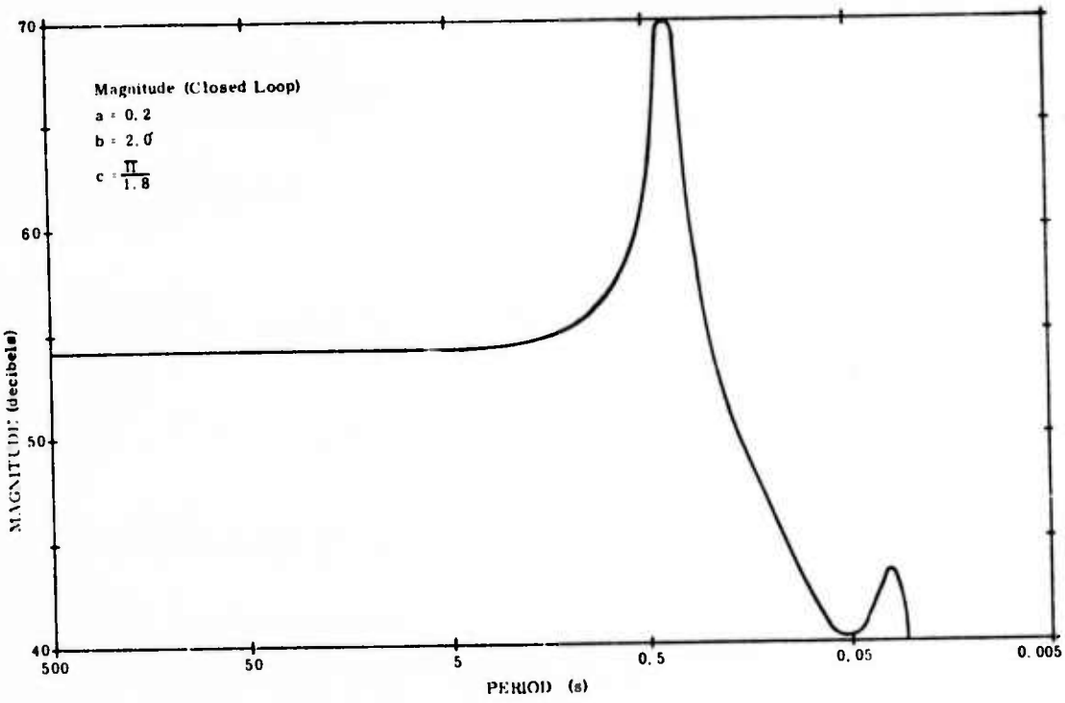

Fig. 3.3-5a Closed Loop Magnitude Response for Binary Seismometer System

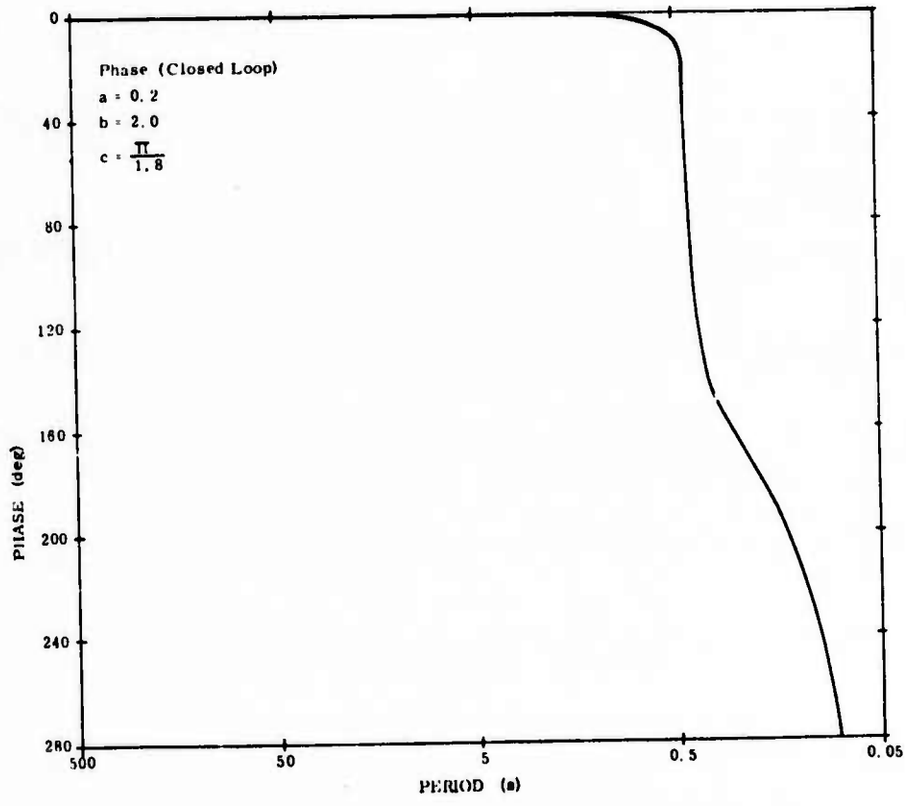

Fig. 3.3-5b Closed Loop Phase Response for Binary Seismometer System

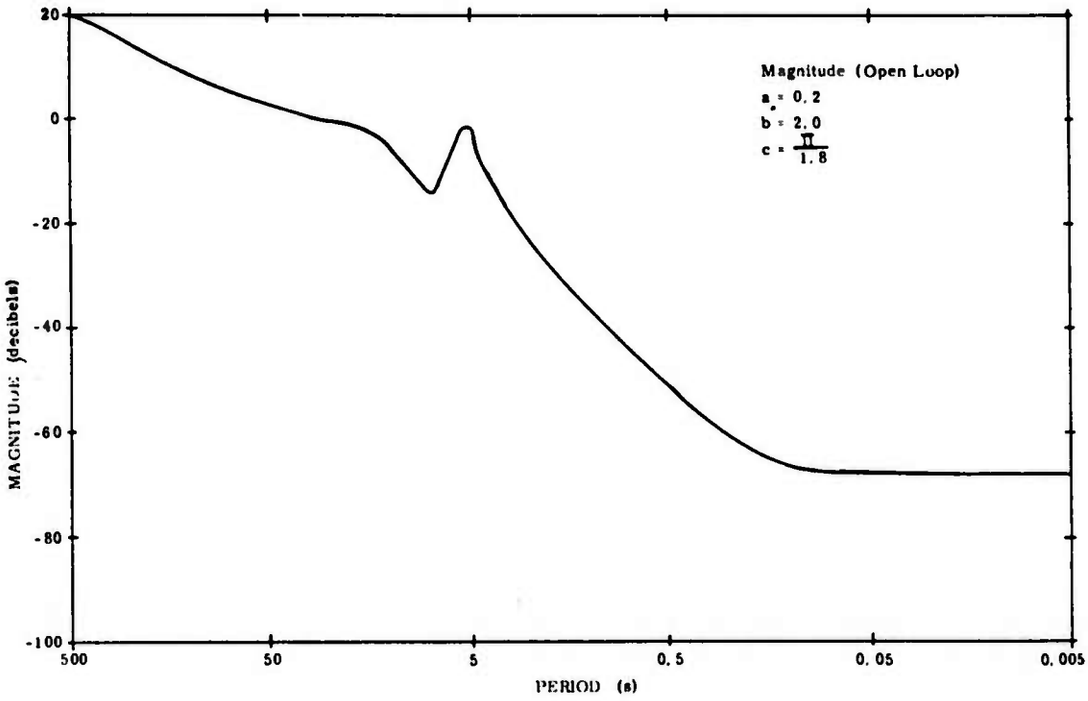

Fig. 3.3-5c Open Loop Magnitude Response for Binary Seismometer System

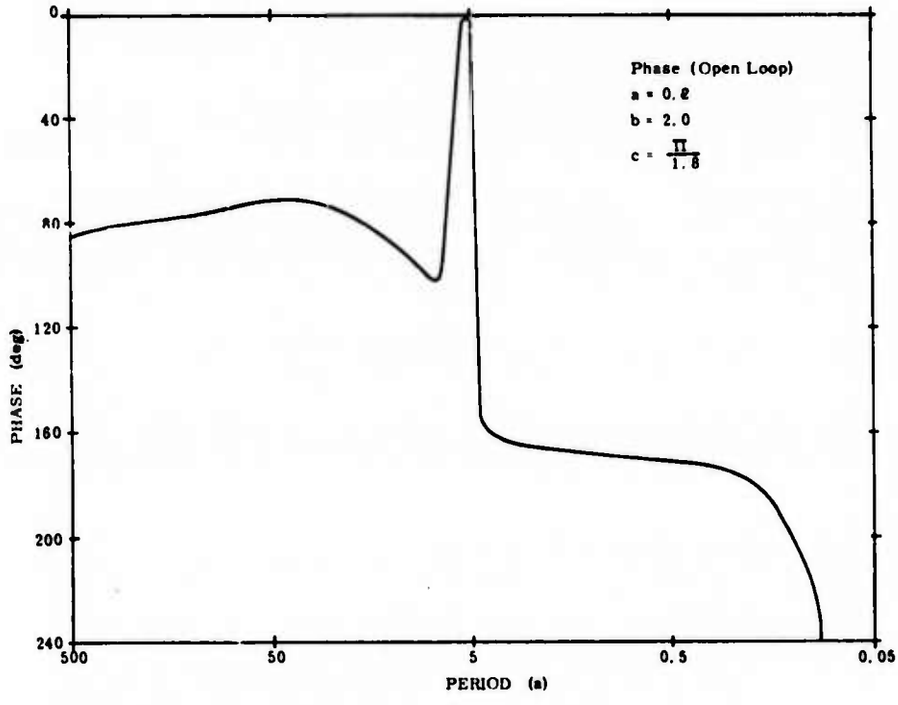

Fig. 3.3-5d Open Loop Phase Response for Binary Seismometer System

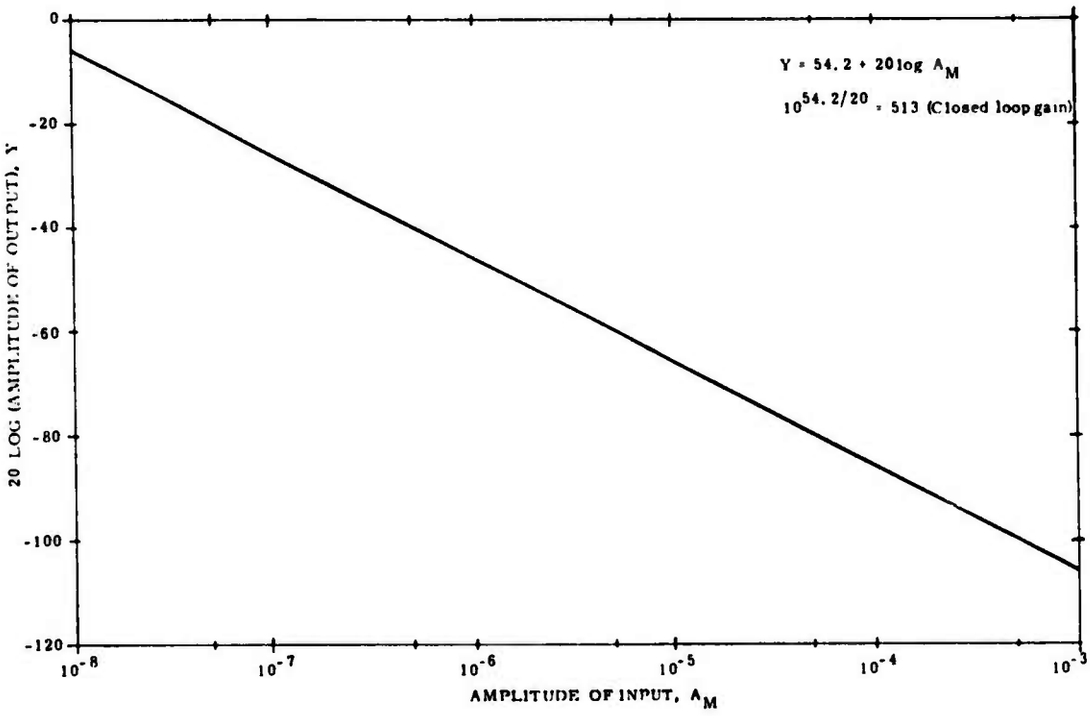

Fig. 3.3-6 Linearity Plot of Binary Seismometer System

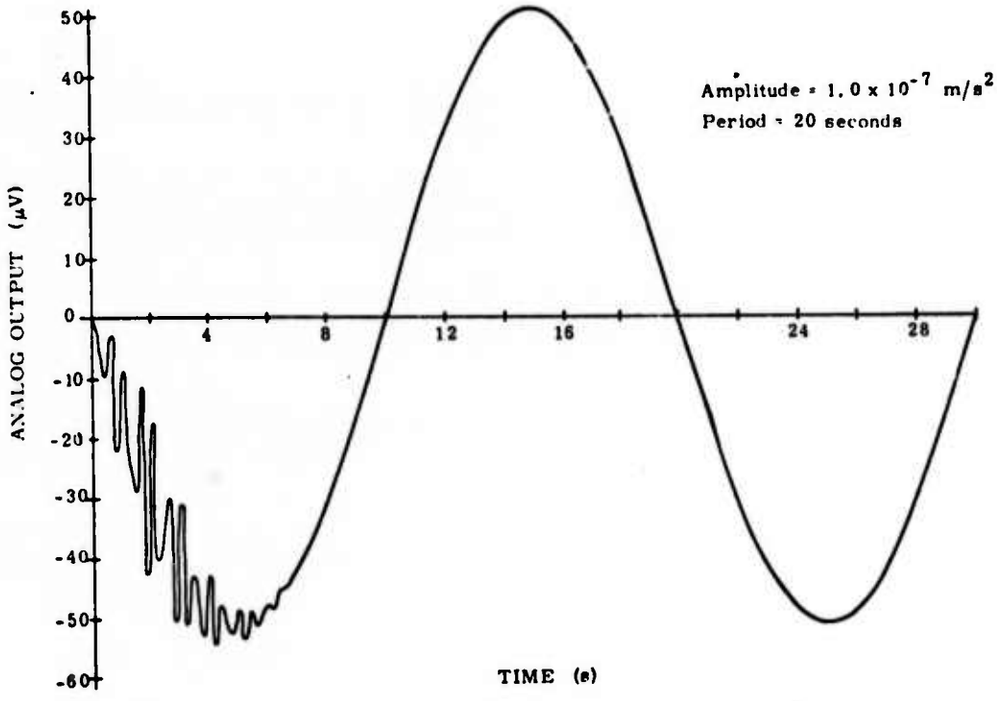

Fig. 3.3-7 Analog Output Waveform for Binary System

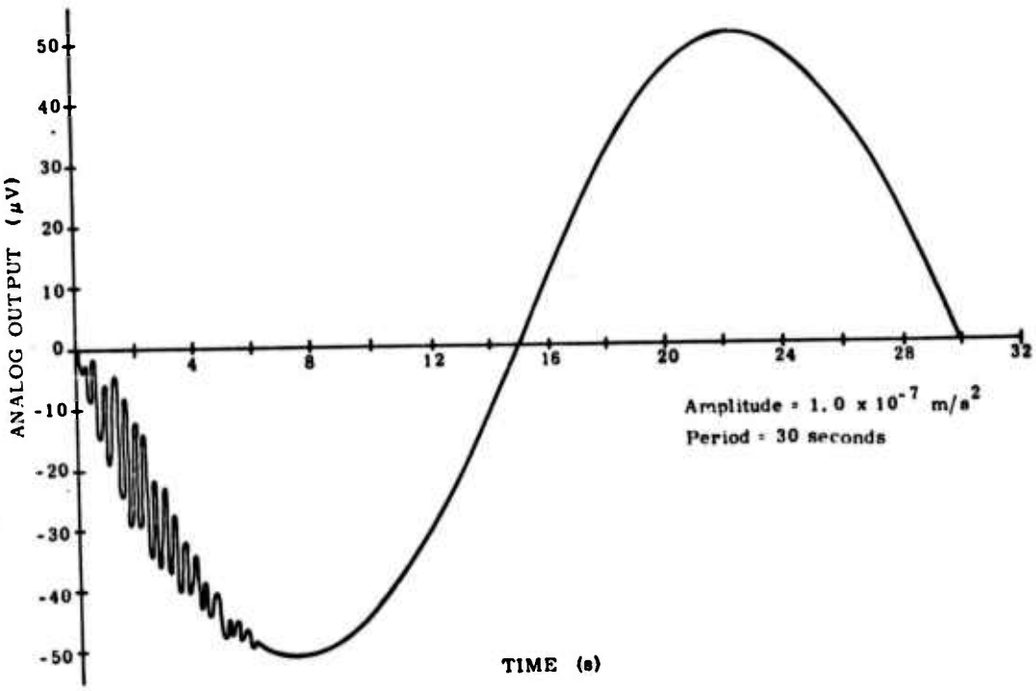

Fig. 3.3-8 Analog Output Waveform for Binary System

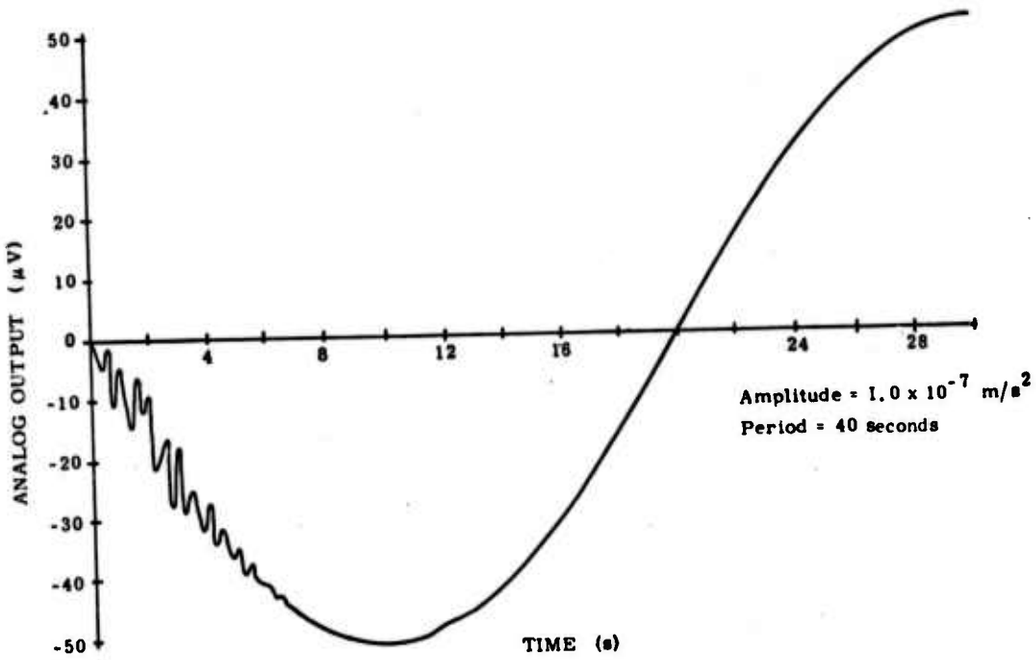

Fig. 3.3-9 Output Analog Waveform for Binary System

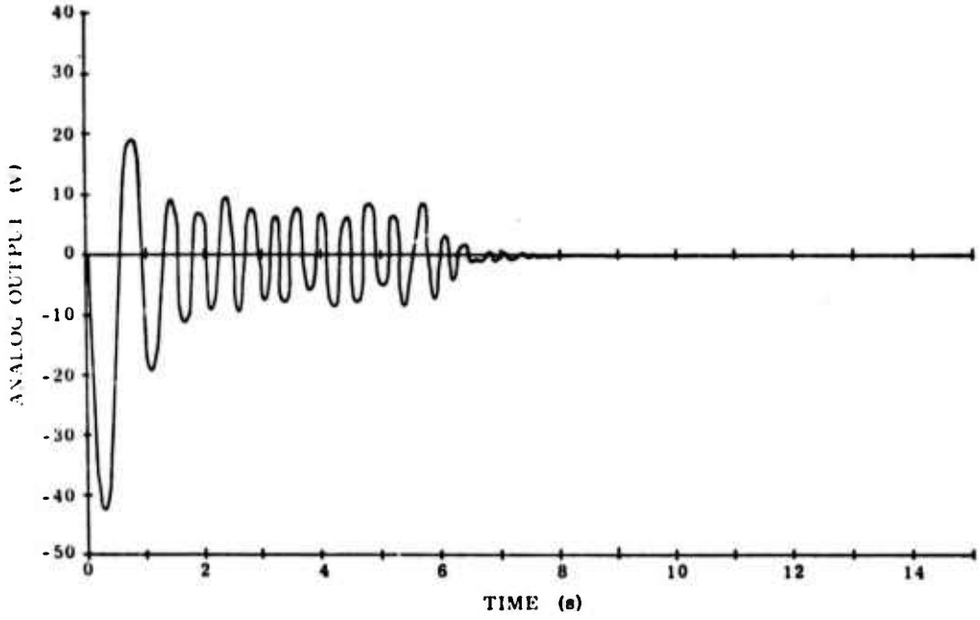

Fig. 3.3-10 Transient Response to Saturating Input

3.4 Linear System with Outboard Analog-to-Digital Conversion

Outboard analog-to-digital conversion implies the use of the linear system in Fig. 3.1-1 with a digitizer attached to the output (see Fig. 3.4-1).

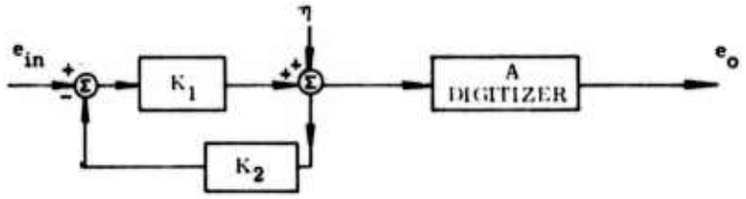

Fig. 3.4-1 Seismometer System with Outboard Digitizer

For simplicity, the feed forward components have been lumped into K_1 and the feedback into K_2. A represents a gain of 1 for the digitizer. Then:

$$e_o = K_1 A\, e_{in}/(1 + K_1 K_2) + \eta A \qquad (3\text{-}11)$$

where:

η = digitizer noise
e_{in} = input
e_0 = output

Let:

δA represent a change in the digitizer gain
δe_0 represent the resulting change in the output.

Then:

$$\delta e_o = K_1 e_{in} \delta A/(1 + K_1K_2) + \eta\delta A \qquad (3\text{-}12)$$

or to first order:

$$\delta e_o/e_o = \delta A/A \qquad (3\text{-}13)$$

i.e., the fractional change in output is equal to the fractional change in the digitizer.

3.5 Quasi-Linear System with Inboard Analog-to-Digital Conversion

The A/D converter is a quasi-linear instrument. Measuring in fixed increments or quanta. For low level signals (approximately one quantum) the output is not proportional to input. A further nonlinear restriction is introduced by the inability of the converter to track rapidly changing signals. This constraint may be incorporated into an analysis by considering the converter a rate limiting device.

The above analysis applies also to the outboard operation. However, there are advantages to placing the digitizer inside the loop, advantages which usually result from feedback networks. Figure 3.5-1 shows a configuration with the digitizer inboard.

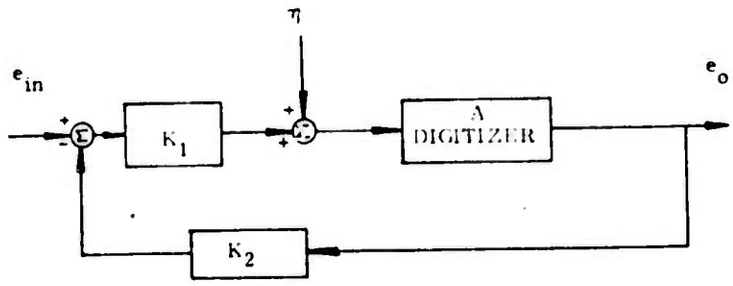

Fig. 3.5-1 Seismometer System with Inboard Digitizer

The relation between output and input is given by:

$$e_o = K_1 A\, e_{in}/(1 + K_1K_2A) + \eta A/(1 + K_1K_2A) \qquad (3\text{-}14)$$

where:

$$A(\text{nominal}) = 1$$

It is apparent from Eq. 3-13 that noise has already been reduced by the factor, $(1 + K_1K_2A)$.

Let:

δA = variation in digitizer gain

δe_0 = effect on the output.

Then:

$$\delta e_o = K_1\, e_{in}\, \delta A/(1 + K_1K_2A)^2 + \eta\delta A/(1 + K_1K_2A)^2 \qquad (3\text{-}15)$$

To first order, the variation in output is given by:

$$\delta e_o/e_o = (\delta A/A)/(1 + K_1K_2A) \qquad (3\text{-}16)$$

Hence, the effect of the percentage variation in A is reduced by the loop gain.

Computer simulations were made for the inboard system with the digitizer placed in the high gain (.02-1) Geotech loop. Step inputs were used ranging in magnitude from 4.0×10^{-10} m/s^2 to 1.0×10^{-7} m/s^2. This interval was chosen to determine the effects of nonlinearities on system response. Overall system gain corresponded to the Geotech value of 1.0×10^5. Five V/s rate limiting in the digitized measurement was used in all the simulations.

Figure 3.5-2 shows the response to a step input of 4.0×10^{-10} m/s. Although the effect of the 10 μV quantum measuring increment is evident, the output has the appearance of the step decay appropriate to an equivalent linear system.

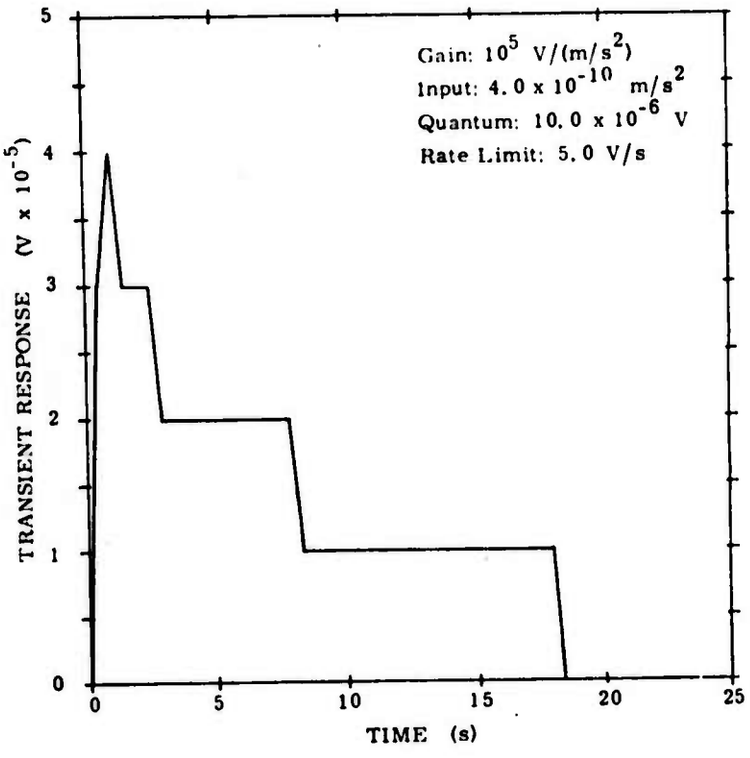

Fig. 3.5-2 Transient Response of Inboard Digitizer to Low Level Step Input

Figure 3.5-3 displays the response to a step input of 1.0×10^{-9} m/s^2 with a quantum of 40 μV. Again the figure has the appearance of a step decay.

Figure 3.5-4 presents the response of the system to a large (relative to the 40 μV quantum) input of 1.0×10^{-7} m/s. The output response appears linear, as the maximum amplitude is several orders of magnitude greater than the quantum of the digitizer.

The acceleration equivalent of a Rayleigh displacement wave is shown in Figure 3.5-5. The curve was derived by taking second differences of the displacement data and using linear fits for continuity. This acceleration equivalent of Rayleigh noise generated the input to the system.

Figure 3.5-6 is the output for the Rayleigh acceleration input. A comparison of the two figures shows good agreement. The effect of the rate limiter is indicated by the smoothing of large rapid changes in signal (5 V/s). A comparison of the two signals was made at the acceleration level rather than at the displacement level since this approach provided a better indication of system performance. Double integration tends to smooth out disparities in comparisons.

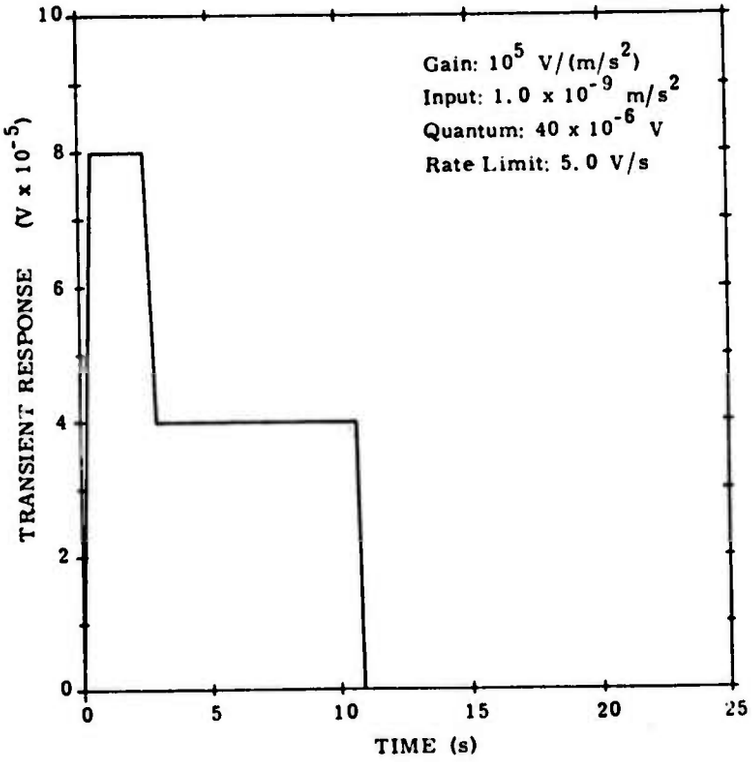

Fig. 3.5-3 Transient Response of Inboard Digitizer to Low Level Step Input

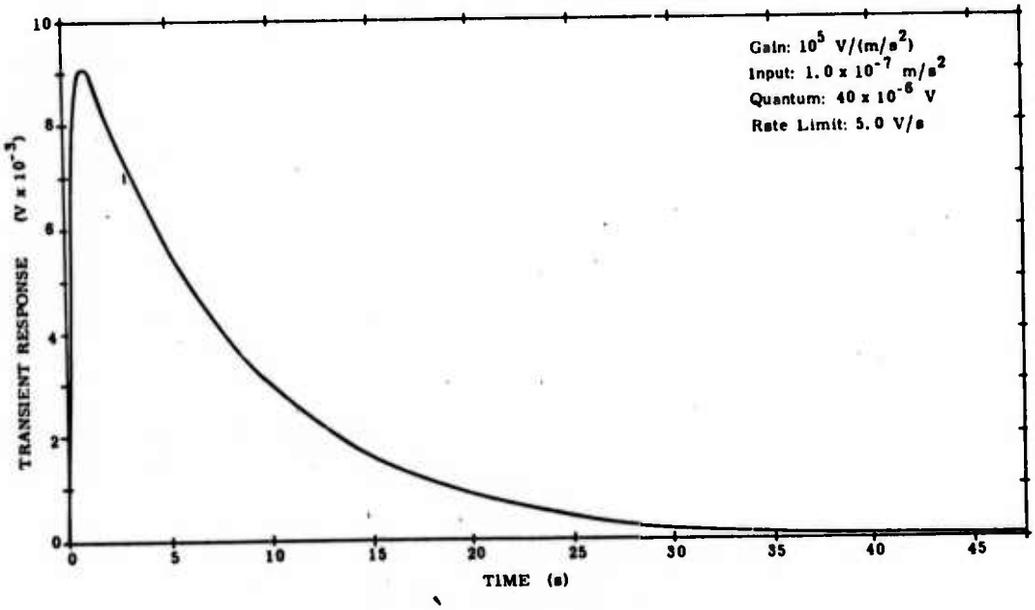

Fig. 3.5-4 Transient Response of Inboard Digitizer to High Level Step Input

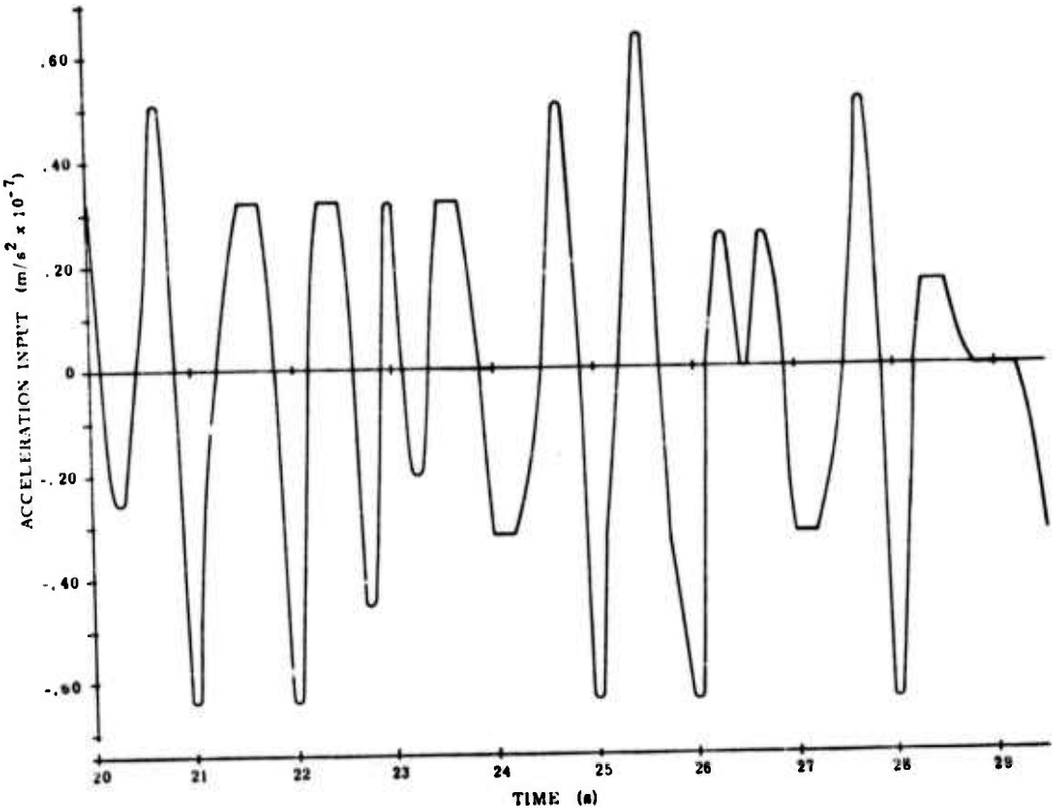

Fig. 3.5-5 Rayleigh Acceleration Wave (Segment)

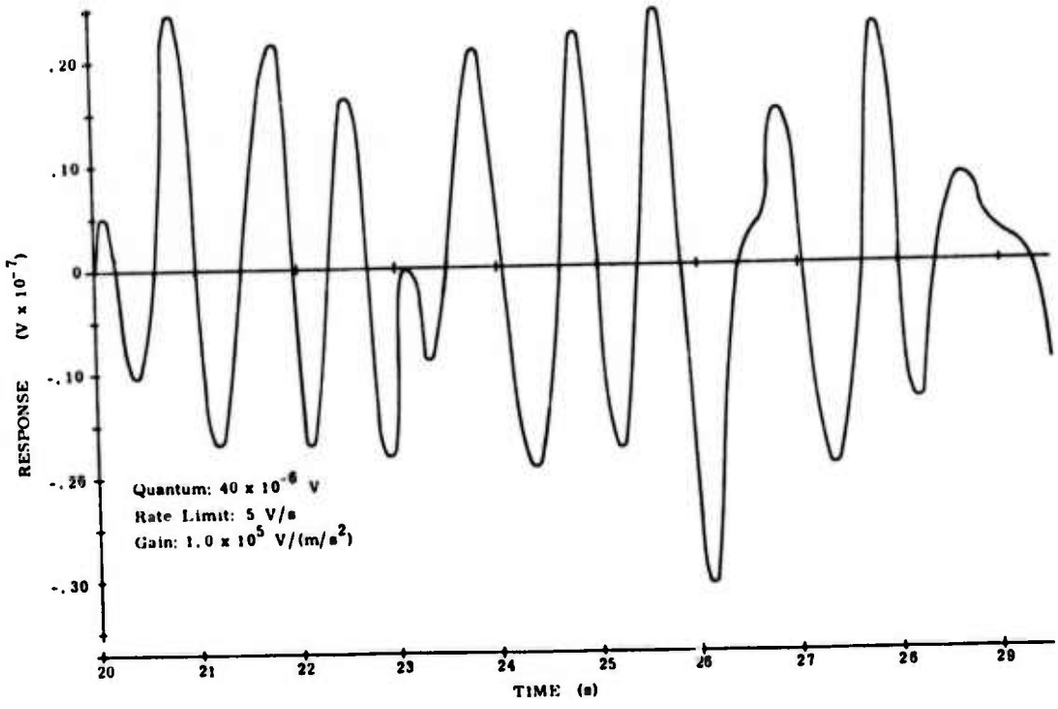

Fig. 3.5-6 Response to Rayleigh Acceleration Wave

CHAPTER 4

ELECTRONICS DESIGN CONCEPT

Within the framework of the theoretical analysis presented in Chapter 3, a basic electronics approach was chosen to meet the desired objectives. A simplified block diagram of this approach is shown in Fig. 4.0-1. With the A/D converter removed the remaining blocks could be configured as in the current Geotech system.

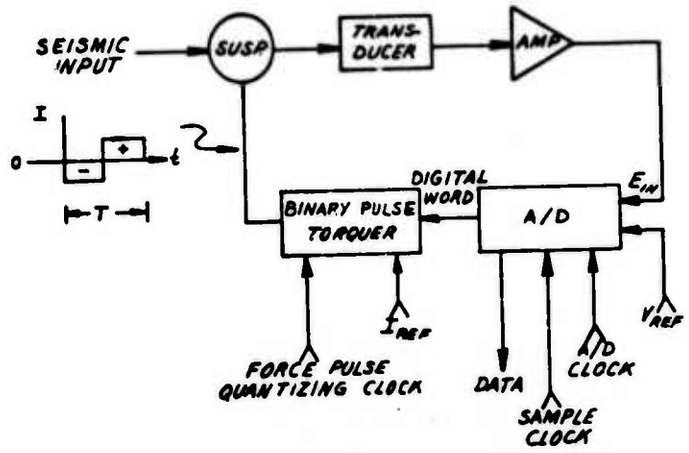

Fig. 4.0-1 Block Diagram of Digital Seismometer Control Loop

The theoretical results indicated that a ternary pulse-torque loop would be unsatisfactory and further loop implementation was terminated.

Since both the pulse width modulated loop and the analog loop (A/D converter within the loop) required equivalent A/D blocks (through the pulsed loop required more rigorous constraints) a study was made of the A/D portion of the loop in generalized form.

An 18 bit A/D converter was chosen for the design. The full range ideally would have been 21 bits to correspond to the seismometer operating goals listed in Chapter 2. However, it was advisable to keep the resultant hardware from becoming overly complex and costly. In addition, the timing requirements of the pulse width modulated loop (0.1 second sample period) required excessively high clock frequencies in the A/D converter if more than an 18 bit A/D converter were considered.

An evaluation of the noise introduced by the A/D circuitry is presented in Chapter 6. This noise level is comparable to that introduced by the analog portion of the loop, and consistent with the design goal of having the instrument noise at 20 db below the lowest anticipated signals to be measured.

CHAPTER 5

SEISMOMETER DIGITIZING ELECTRONICS ANALYSIS

5.1 Introduction

The object of this chapter is to analyze the errors and problems associated with the analog-to-digital converter in a generalized form. The analysis splits the A/D converter into four sections:

(1) Voltage Reference and Scaler
(2) Ladder and Switch
(3) Amplifiers, Sample and Hold, and Comparator
(4) Logic and Timing

A representative design for each section will be chosen and analyzed. The errors will be broken into static errors which can be adjusted to zero during test and compensatable errors such as temperature coefficients and nonlinearities.

5.2 Voltage Reference and Scaler

5.2.1 Voltage Reference

The less stringent scale factor accuracy requirements for this A/D converter relative to that in a gyro loop, make it possible to amplify the basic 6 V PVR type reference used in the CSDL SIRU system to about 10 V, using an operational amplifier. This will introduce some static errors which, however, should be stable. This will also allow relatively high loads on one reference, since the output impedance will be essentially zero. A 10 V level was picked as a good compromise between the expected input signal range to the A/D converter and the probable use of a ±15 V bus for the amplifiers. Voltage references other than PVR's could be used. However, in this prototype stage it is advisable to use a better reference and then back-off after gaining test experience.

5.2.2 Scaler

There are two ways to implement the requirement for reference scaling between the lower and upper order bits. One is to scale the reference as applied to the resistance ladders. This would involve a simple resistor divider. The second is to use the same reference voltage for both ladder sections, but scale their outputs

by the gain and summing resistors in the comparator section. The second method is more desirable since it allows for finer adjustment with higher value resistors and also avoids output impedance problems associated with a reference divider. It also places all the critical adjustments required for the A/D converter in the same location, the input stage. Thus for this analysis a single value reference will be assumed and scaling will be done in the comparator stage.

The basic implementation is shown in Fig. 5.2-1. Typical components would be: Vishay type S102 resistors, Harris HA 2904 operational amplifier, load compensated SIRU PVR and a good grade mylar capacitor. For these components:

$R_2/R_1 \approx 1.6$ (to obtain 10 volts output)

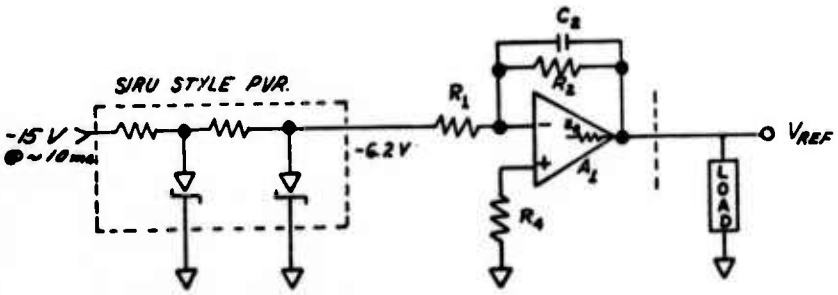

Fig. 5.2-1 Voltage Reference Circuit

Let:

$R_1 = 10 \quad k\Omega$
$R_2 = 16.0\ k\Omega$

Select a value of C to give approximately a 100 Hz low pass filter. This will remove some of the noise inherent in the resistors, amplifier and PVR. The required value of C is given by:

$$C = \frac{1}{2\pi fR} \cong .1\mu F \qquad (5\text{-}1)$$

5.2.3 Summary of Voltage and Scaler Errors

The errors for the voltage reference and scaler are:

Static	
Tolerance	1.01%
Offset	57.1 μV
Compensatable	$\pm 20\ \mu V/^{o}C$

See Appendix A for a more detailed discussion.

5.3 Ladder and Switch

Ladder networks of the required accuracy are available only to 12 bits. Thus the ladders and switches will be broken into two sections (see Fig. 5.3-1). The main problem with this technique is to maintain a monotonic summation of the two ladder outputs.

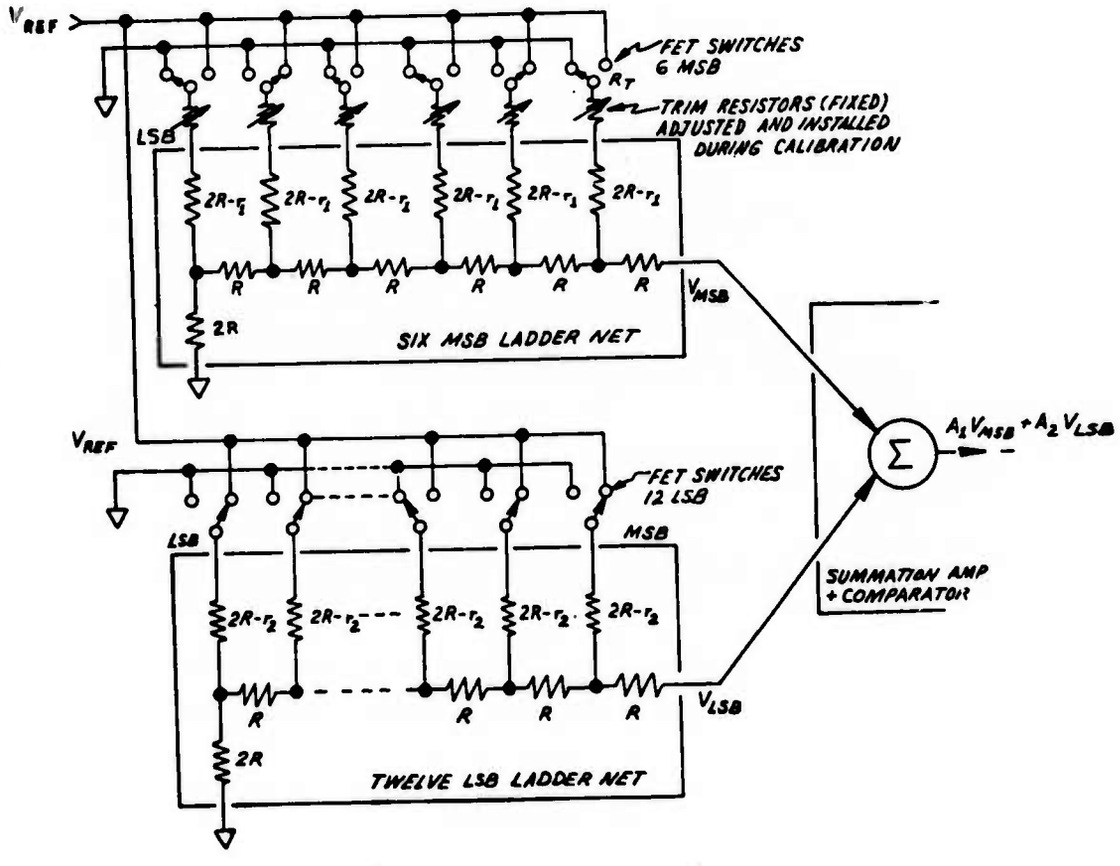

Fig. 5.3-1 Ladder Networks

Figure 5.3-2 shows the outputs of the two ladders graphically. The ladder networks are divided into a least significant bit 12 (LSB) ladder and a 6 MSB ladder to allow adjusting for monotonicity and linearity more easily. The 6 bit ladder has a small resistance subtracted from each leg to allow adjusting for the "on" resistance of the FET switch to insure monotonic behavior.

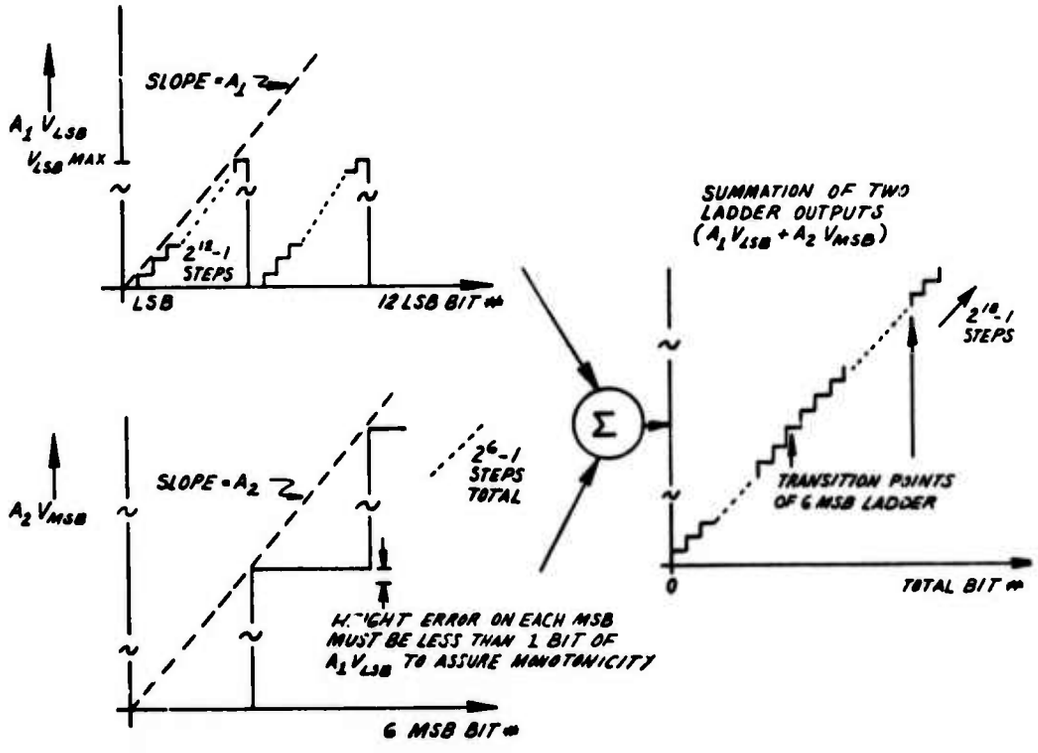

Fig. 5.3-2 Graphical Representation of the Ladder Outputs

A_1 and A_2 are gains in the summation amplifier and comparator that provide linearity adjustment. For the ladder analysis, A_1 and A_2 are assumed to be unity. Gain effects will be discussed in the next section. Overall errors will depend primarily on the initial calibration and are hard to estimate. However, the calculations will show the approximate values involved.

5.3.1 Monotonic Requirements

The requirements for monotonicity of the ladder networks can be examined as follows:

a) 6 MSB: ASSUME R (Fig. 5.3-1) equals 10 kΩ and r_1 equals 100 Ω. Assume the use of a Siliconix DG190A switch with a maximum "on" resistance of 30 Ω; also that R_T can be trimmed to within 0.1 Ω over a range from 70 to 100 Ω.

Under these conditions the maximum error in the height of V_{MSB} will be:

$$10V \left(\frac{1}{2} - \frac{2R}{4R-r_1+R_T+R_{DS-on}}\right) = 10 \left(\frac{1}{2} - \frac{20,000}{40,000 \pm 0.1}\right)$$
$$= \pm 12.5\mu V$$

The height of one step in the 12 LSB will be:

$$\frac{10.0}{2^{18}} = 38.1\mu V$$

Thus under the worst case of the highest order bit, monotonicity should be attainable. The above adjustment also compensates for the initial matching tolerances of R in the ladder (typically .01 to .1%).

b) 12LSB: ASSUME R equals 10 kΩ and r_2 equals 30 Ω. Assume the same switches are used as for the MSB ladder and that the R_{DS-on} match is ±10%.

Under these conditions the maximum error in LSB height will be:

$$\frac{10}{2^6} \left(\frac{1}{2} - \frac{2R}{4R-r_2+R_{DS-on}}\right) = \frac{10}{64} \left(\frac{1}{2} - \frac{20,000}{40,000 \pm 3}\right)$$
$$= \pm 5.8\mu V$$

Thus the lower 12 bits will be monotonic without further adjustment.

5.3.2 Temperature Coefficients

Typical temperature coefficient (TC) tracking within the ladders is 1 ppm/^{o}C. This will result in a worst case TC of 10 μV/^{o}C on the MSB of the ladder. Because the ratiometric technique is used, absolute TC of the ladders (±50 ppm/^{o}C) has negligible effect. Switch $R_{DS\text{-}on}$ TC is typically 0.2 Ω/^{o}C. Thus the TC of the MSB is:

$$\frac{10}{64}\left(\frac{1}{2} - \frac{20{,}000}{40{,}000 \pm .2}\right) = \pm 5.8\mu V$$

The switches will track each other typically to about 10%. Therefore monotonic behavior will be assured over the temperature range. The TC will change only the overall scaling. Any TC mismatch between ladders will also cause a small nonlinearity in the overall slope. The TC of the trim resistors should introduce no significant errors.

5.3.3 Tolerance

Tolerance in the initial value of R in the ladders will cause only second order effects since the R - 2R technique is ratiometric.

5.3.4 Leakage

Typical switch leakage at 50^{o}C is about .4 nA per switch. The ladder never senses these leakages because the SPDT switches shunt them to V_{REF} or to ground (see Fig. 5.3-3).

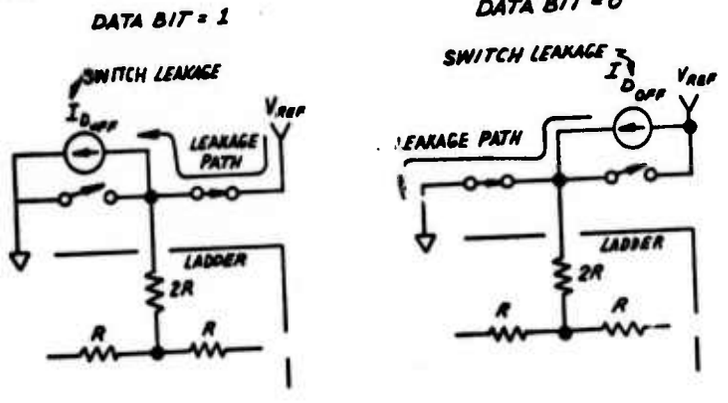

Fig. 5.3-3 Switch Leakage Paths

5.3.5 Switch Transient

The worst case switch transient occurs when the MSB is switched. The magnitude of this "spike" is determined primarily by the RC product of the ladder R and the switch capacitance (see Fig. 5.3-4). The worst case transient actually depends on the initial charge states of the various capacitors, but for this approximate analysis the initial conditions are assumed zero. The time constant, τ, can be computed by:

$$\tau = (C_{D\ off} + C_{S\ on} + C_{D\ on}) \times 4R \qquad (5\text{-}2)$$

$$\tau = 19pF \times 40\ k\Omega$$

$$\tau = .76\ \mu s$$

Therefore the time for the output to settle to less than 1 LSB error (38 μV) is:

$$t = \tau \ln \left[\frac{V_{REF}}{V_{LSB}} \cdot \frac{2R}{4R}\right] \qquad (5\text{-}3)$$

$$t \cong 9\ \mu s$$

This time would limit the frequency of the A/D clock to about 110 kHz. To speed up the clock, either R of the ladder must be lowered, which would require a more precise adjustment of R_T, or else a shunt should be placed from the switch common to ground. The latter method is more practical.

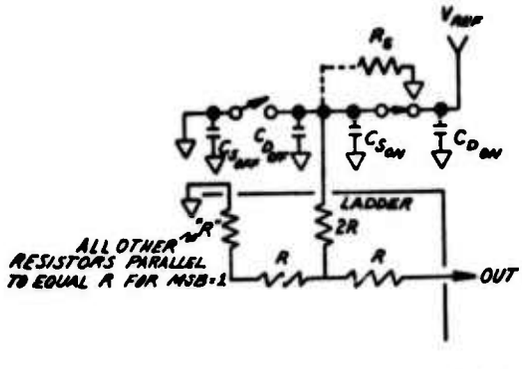

Fig. 5.3-4 Portion of Ladder Network Determining Switch Transient Response

Assuming a 10 kΩ shunt (R_S in Fig. 5.3-4), the time required to obtain less than 1 LSB error is about 2.3 μs. Therefore, if the comparator is strobed at some time greater than 2.3 μs after the switch command, the transient would introduce less than 1 LSB error (Fig. 5.3-5).

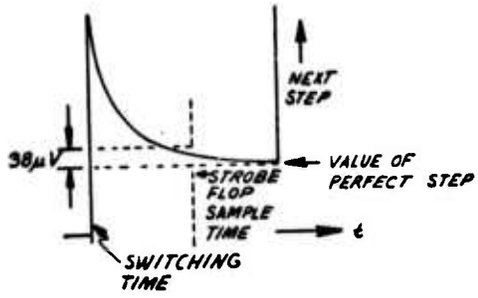

Fig. 5.3-5 Output of Ladder Step

5.3.6 Circuit Delays and Maximum Slew Rate

Circuit delays will also be present. These will consist of:

1) ladder settling	250 ns, typical
2) switch risetime	100 ns, typical
3) switch deadtime	60 ns, typical
4) switch drive logic risetime	25 ns, typical
Total delay	435 ns, typical

The total delay time should be added to the strobe delay time giving a total strobe delay of about 2.8 μs. Assuming the strobe time is step centered the total strobe delay will allow step times of about 5 μs. Therefore, the ladder will track a maximum input envelope slew rate of about 38 μV/5 μs = 7 V/s.

5.3.7 Summary

Because of the adjustable nature of the ladder and switch section exact prediction of the error is difficult. However, it appears that the circuit and components can achieve the required rate, linearity and monotonicity. It should be noted that the necessity of ensuring monotonic behavior sets an upper bound on the nonlinearity error of the two ladders. The remaining nonlinearity will be determined by the gain errors in the amplifiers used to combine the two outputs and the temperature

coefficients discussed above.

5.4 Amplifiers, Sample and Hold, and Comparator

5.4.1 Input Amplifier

The input amplifier must scale the input signal, E_{in}, offset it to allow a single ended output, offset any static errors and provide a low impedance drive for the following stages (see Fig. 5.4-1). A high frequency rolloff capacitor is also shown to allow reduction of any logic generated noise.

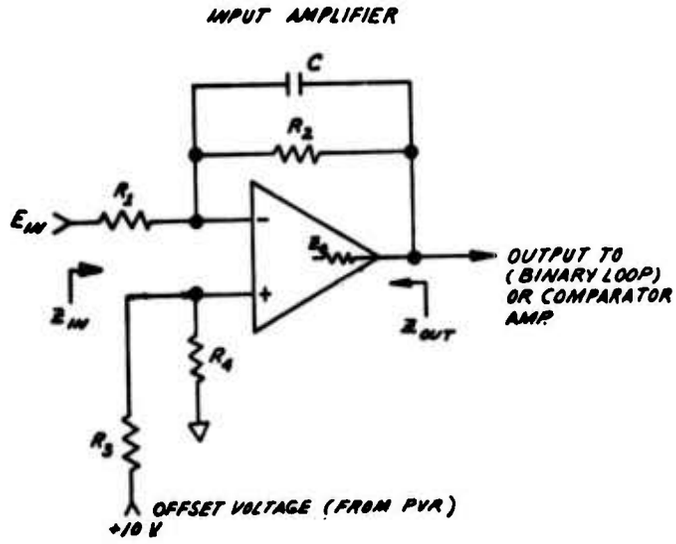

Fig. 5.4-1 Input Amplifier Circuit

Although the amount of offset and gain necessary in this stage varies with loop configuration it will not exceed unity (-1) gain, and the offset probably will not exceed 10 V. Therefore as a worst case, unity gain and 10 V offset will be considered. Offsets of less than 10 V can be implemented by changing the (+) input gain (adjusting R_3 and R_4). Precise seismic input gain is adjusted with R_1 and R_2. The high frequency rolloff occurs at frequencies that do not affect the stability criteria of the loop, and it need not be computed, since its exact value will be determined empirically.

As before, an HA2904 amplifier and Vishay S102 resistors are assumed. To prevent loading of the preceeding stages in the seismic amplifier, R_1 is assumed = 10 kΩ. The output impedance, Z_{out}, may be computed from the following relationship:

$$Z_{out} \doteq \frac{Z_0}{1 + \frac{A}{(1 + \frac{R_2}{R_1})}} \qquad (5\text{-}4)$$

where A is the open loop gain. For the HA2904, $A = 5 \times 10^8$, typically, and $Z_0 = 200\Omega$. Therefore $Z_{out} \approx 0$.

5.4.1.1 Slew Rate

The maximum slew rate of any expected input signal is 96 V/sec. (or $96\mu V/\mu s$). The HA2904 slew rate is specified as 2.5 $V/\mu s$. Therefore no error is expected.

5.4.1.2 Summary of Input Amplifier Errors

Assuming unity gain and 10V offset the errors for the input amplifier are:

<u>Static Errors</u>	
Tolerance	.02%
Offset	42 μV
<u>Compensatable Errors</u>	
Signal Gain	± 1.5 ppm/^oC
Offset Gain	± 1.5 ppm/^oC
Amplifier Offset	± .8 $\mu V/^oC$

As in the reference case, the static errors can be trimmed out. See Appendix B for a more detailed discussion.

5.4.2 Sample and Hold

In the case of a binary force rebalance loop, a significant ripple component will be present on the input signal to the loop, caused by the 10 Hz current pulses. Computer simulation has shown that the maximum slope of the ripple component at the digitizing time is 96 V/s (see Fig. 3.3-4). The A/D converter cannot follow this fast a signal, even in a successive approximator configuration. Thus it would be necessary to sample and hold the input signal to allow an A/D conversion if the

binary loop were to be used.

If a tracking A/D converter is used, the time to convert depends on the size of the change from sample to sample with an envelope slew rate of 4 V/s. This change can be .4 V, which is equivalent to 10,000 counts. With a clock frequency of 200 kHz a maximum of 50 ms, would be needed. Clearly, a tracking configuration cannot be used without causing large, highly variable errors and loop instability.

Assuming a successive approximating A/D converter is used, a maximum of 90μs would be needed to convert to 18 bits, assuming the converter resets after each conversion. If a tracking successive approximator is used (i.e., the A/D converter remembers the previous conversion and starts from there at each sample), the maximum deviation from sample to sample will be 14 bits, requiring only 70 μs to convert. This would be the fastest configuration to get the required resolution on a 4 V/s envelope. The penalty is relatively complicated logic. The following analysis will attempt to design the sample and hold and to analyze its errors for this configuration. The model shown in Fig. 5.4-2 will be used.

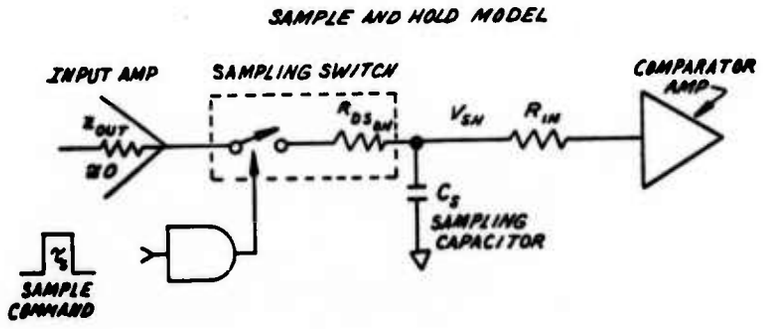

Fig. 5.4-2 Sample and Hold Circuit

Assume the turn-on transients have decayed to a negligible level and the sample and hold is sensing only a .4 V maximum change from sample to sample (every 0.1 second). Further assume the sampled input value is 10V. In order for the error during the conversion time, $\tau_{A/D}$, to be less than 1 bit or 38 μV (see Fig. 5.4-3), the RC time constant required is computed by:

$$|\text{error}| = V_{in}\left(1 - e^{-\frac{t}{R_{in}C_S}}\right) \qquad (5\text{-}5)$$

or

$$R_{in} C_S = - \frac{t}{\ln (1 - \frac{error}{V_{in}})}$$

Therefore:

$R_{in} C_S \approx 18.4$ seconds.

Assume we meet this requirement. The decay can now be calculated by:

$$decay = V_{in} (1 - e^{-\frac{t}{R_{in} C_S}}) \qquad (5\text{-}6)$$

where:

$\tau = .1$ second

$V_{in} = 10$ V

Therefore:

decay $\approx .054$ V

Thus if the maximum seismic signal change from sample to sample is .4 V, the maximum the sample and hold will sense is .454 V. The sampling aperture is selected so that less than 1 bit of error will be introduced during the sample time. Since the maximum ripple slew rate at the sample time is 96 V/s, to sample with less than 1 bit of error the sample time, τ_S, would be:

$$\tau_S \leq \frac{38 \mu V}{96 \text{ V/s}} \cong 396 \text{ ns}$$

Let $\tau_S = 500$ ns. This will allow for the rise and fall times of the switch. Using the computed input change to the sample and hold between samples (.454V), the value of C_S to allow charging to within 38 μV (1 bit) of the correct value in τ_s can be computed (see Fig. 5.4-4). The minimum resistance through which C_S can be charged is R_{DS-on}. Assuming use of a DG190A, R_{DS-on} is 30 Ω. Thus C_S can be computed by:

$$|error| = \Delta V_{in} e^{-\frac{t}{R_{DS-on} C_S}} \qquad (5\text{-}7)$$

where:

$$t = \tau_S$$

$$\Delta V_{in} = .454V$$

$$C_S = - \frac{\tau_S}{R_{DS-ON}^{IN}} \quad \frac{error}{\Delta V}$$

$$C_S \simeq 1775 \text{ pF}$$

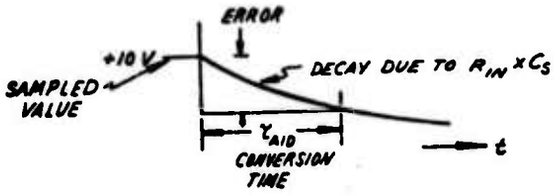

Fig. 5.4-3 Signal Decay During A/D Conversion Time

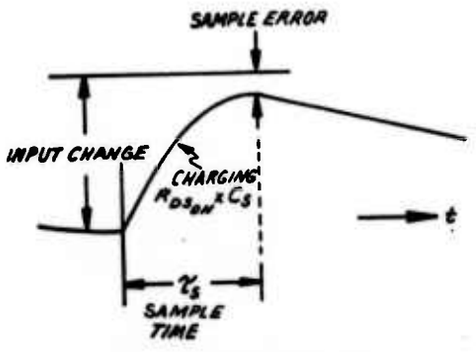

Fig. 5.4-4 Sampling Error

R_{in} is then computed by:

$$R_{in} C_S = 18.4$$

$$R_{in} \simeq 10^{10} \Omega$$

This high value for R_{in} is impractical, especially for a fast enough I.C. amplifier to allow a correct comparison to be made.

It should be noted that this analysis is somewhat optimistic in assuming the ripple component slew rate does not change. In reality this will not be the case. The 96 V/s value was generated from a simulation assuming 50% duty cycle of the binary input pulse. For duty cycles corresponding to large dynamic excursions,

the slope will change radically. Furthermore, effects of leakage current and offset associated with such high values of R_{in} would also introduce large errors. Input offset currents of the comparator alone would introduce temperature coefficient errors of greater than .5 V/^{o}C (or > 13 bits/^{o}C). Even if the $10^{10}\,\Omega$ value for R_{in} could be achieved, a large nonlinearity would still result, thus negating any advantages achieved by the relatively complicated tracking successive approximation technique.

If other sampling techniques are used, such as peak detectors, the loop errors would still be high since leakages would still dominate because of the high impedances necessary to obtain the accuracy during the conversion time. A peak detector would also force the A/D conversion to be performed after the occurrence of the peak signal. This would require a conversion to occur during the succeeding force rebalance pulse, thus restricting the dynamic range.

In conclusion the excessive speed and accuracy problems associated with the large ripple component make the binary force rebalance loop extremely difficult to implement. It should be repeated that this restrictive sample and hold design is necessary only for the binary rebalance method. Any approach not having the large ripple component would yield a sample and hold circuit that was readily achievable (if it were necessary at all).

5.4.3 Comparator Amplifier

The comparator amplifier, Figs. 5.4-5 and 5.4-6, must receive the offset adjusted input signal (or the sample and hold output) and compare it to the summation of the ladder outputs to provide a logic command indicating either the equality or the larger of the two inputs. It also must have a slight amount of hysteresis or dead band to prevent noise induced oscillation about its final value.

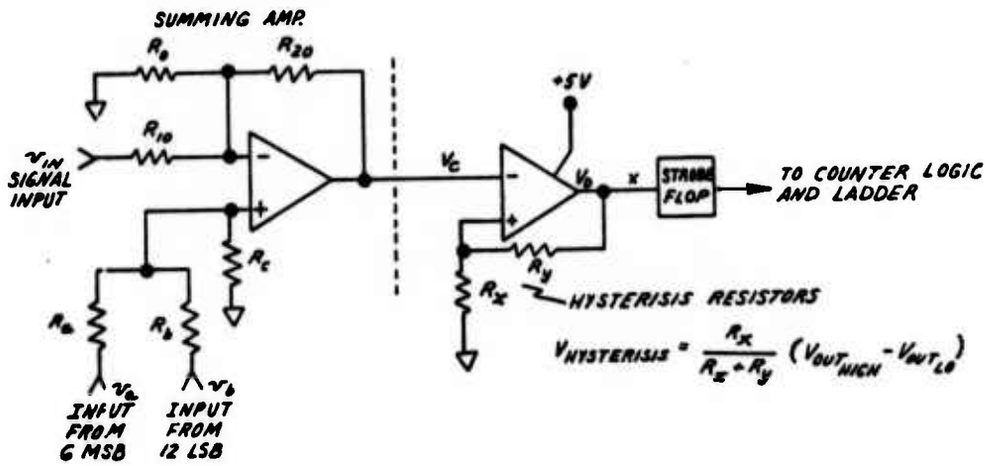

Fig. 5.4-5 Comparator Amplifier: Convert and Hold Type

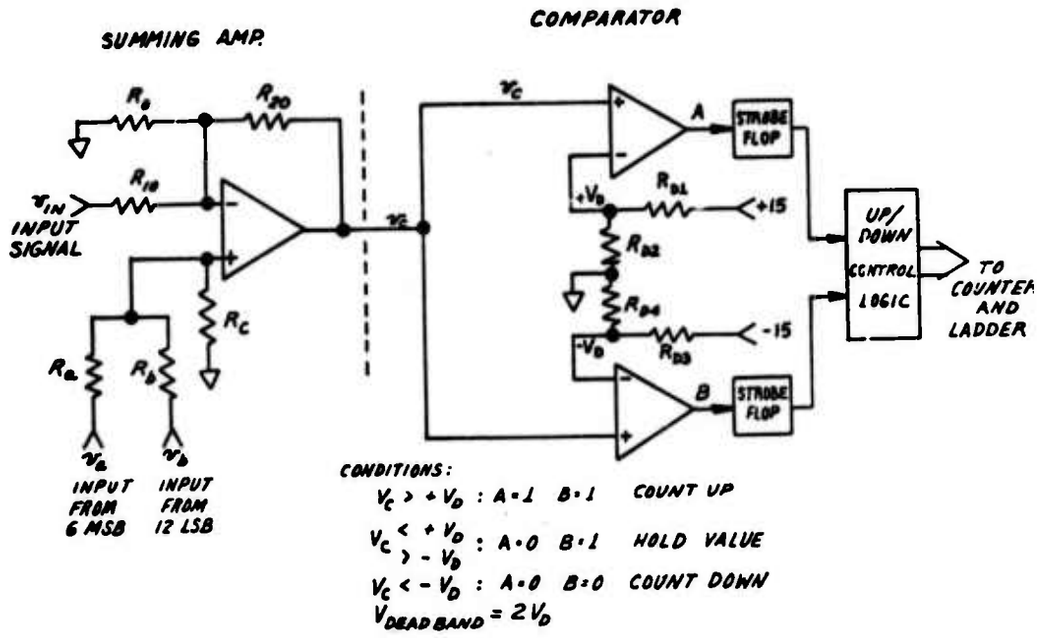

Fig. 5.4-6 Comparator Amplifier: Tracking Type

Two configurations are possible depending on whether or not the A/D converter must track. Though it is possible to combine the functions of the summing amplifier and the comparator into one stage, this analysis assumes a separate summing amplifier to allow more flexibility of adjustment. For both amplifier - comparator configurations the summing amplifier is the same.

5.4.4 Summing Amplifier

Assume a required unity gain for both the input signal and the combined ladder input, and a scaling of the 12 LSB input to the 6 MSB by a gain of $1/2^6$ or .015625. Figure 5.4-7 then shows a generalized differencing amplifier. Given the

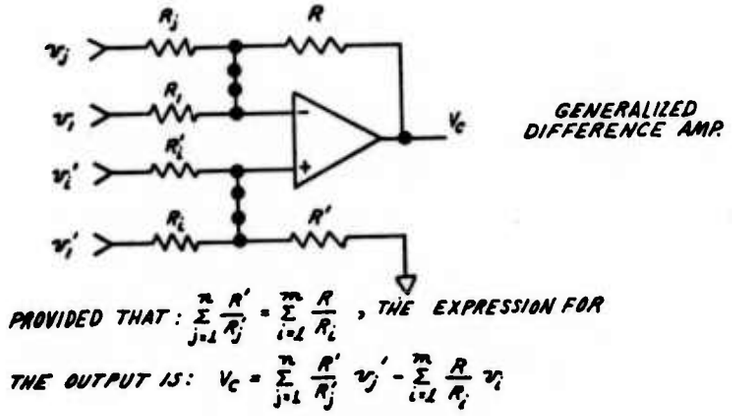

Fig. 5.4-7 Generalized Difference Amplifier

resistance ratio constraint as:

$$\sum_{j=1}^{n} k'_j = \sum_{i=1}^{m} k_i \qquad (5\text{-}8)$$

where:

$$k'_j = \frac{R'}{R'_j}$$

$$k_i = \frac{R}{R_i}$$

the expression for v_c is given by:

$$v_c = \sum_{j=1}^{n} k'_j v'_j - \sum_{i=1}^{m} k_i v_i \qquad (5\text{-}9)$$

For the case of two non-inverting inputs, one signal inverting input and one grounded inverting input, (shown in either Fig. 5.4-5 or 5.4-6):

$$v_c = k_a v_a + k_b v_b - k_{in} v_{in} - k_0 \cdot 0$$

or:

$$v_c = \left(\frac{R_c}{R_a}\right) v_a + \left(\frac{R_c}{R_b}\right) v_b - \left(\frac{R_{20}}{R_{10}}\right) v_{in} \qquad (5\text{-}10)$$

where:

$$k_a + k_b = k_{in} + k_0$$

or

$$\frac{R_c}{R_a} + \frac{R_c}{R_b} = \frac{R_{20}}{R_{10}} + \frac{R_{20}}{R_0}$$

The use of the grounded inverting input resistor is necessary to allow the resistor ratio constraint to be soluble for unity signal and ladder gains.

For unity signal gain, $\frac{R_{20}}{R_{10}} = 1$. The corresponding scaling on the ladder inputs is therefore:

$$\frac{R_c}{R_a} = 1$$

$$\frac{R_c}{R_b} = \frac{1}{2^6} = .015625$$

If:

$$R_{20} = R_c = 10\ k\Omega$$

then:

$$R_{10} = R_{20} = R_a = R_c = 10\ k\Omega;$$
$$R_b = 640\ k\Omega$$
$$R_0 = 640\ k\Omega$$

5.4.4.1 Output Impedance and Slew Rate

As in the case of the input amplifier, $Z_{out} \approx 0$ and the slew rate is high enough to contribute negligible errors.

5.4.4.2 Summing Amplifier Error Summary. The errors for the summing amplifier are:

Static

Tolerance	.03%
Offset	42 μV

Compensable

Signal Gain	±1.5 ppm/^{o}C
Ladder Gain	±1.5 ppm/^{o}C
Amplifier Offset	± .8 μV/^{o}C

As before the static errors can be trimmed out. See Appendix C for a more

detailed discussion.

5.4.5 Comparator

The two comparator configurations are shown in Figs. 5.4-5 and 5.4-6. Of the two, the latter will have the higher errors because of the need for two comparators to get the extra logic information. Assuming we want the threshold band to be ± 1 LSB, then $2V_D$ = 76 μV. This value is generated by the dividers off the supply. Let $R_{D1} = R_{D3}$ = 1 MΩ. Then:

$$2V_D = \left[\frac{R_{D2} + R_{D4}}{R_{D1} + R_{D2} + R_{D3} + R_{D4}}\right] \times 30V \qquad (5\text{-}11)$$

$$2V_D = 76\mu V$$

Computing R_{D2} yields:

$$R_{D2} = 2.4\ \Omega$$

Any error in this value will generate only a second order effect in the comparator error and will be negligible. The deadband will also be easily adjustable.

Errors due to input current sources will also be negligible since the output impedance of the preceeding stage is essentially zero. Errors due to input offset voltage, although high in magnitude, can be nulled out by proper adjustment of R_{D2} and R_{D4}, or by offsetting the preceeding stage. It is assumed that LM 106 comparators will be used.

5.4.5.1 Summary Comparator Errors. The errors in the comparators are:

Input Voltage Offset	
.5mV X 2	= 1.0 mV
Input Offset TC	
2 X 3 $\mu V/^oC$	= 6 $\mu V/^oC$

Response Time

The response time of the LM 106 is typically less than 100 ns for 2 mV overdrive and therefore no speed errors will be introduced.

5.4.6 Summary

The errors introduced by the amplifiers and comparators all are well within the limits allowable to design an accurate 18 bit converter. The sample and hold errors, however, are not. Thus any binary force rebalance design should be avoided. Not mentioned in any of the above calculations are power supply errors. The rejection ratios of all the components used are high enough to ensure negligible power supply induced errors for any reasonable power supply design.

5.5 Logic and Timing

Logic and Timing circuits for this application do not present any difficulty. The only critical area in the design is in the speed of the 18 bit counter that drives the ladder. For any tracking approach, low power TTL or CMOS would probably have sufficient speed. If a successive approximator is used, the counter would have higher speed requirements, forcing the use of standard power TTL.

For the binary force rebalance approacn, the logic would be more complicated and would require a high frequency, quantizing clock at about 2.6MHz which would have to be crystal controlled. Other approaches do not require frequencies higher than about 200 kHz and the frequency stability of the oscillator used would not affect the accuracy of conversion. Another complexity which the binary technique imposes is the need for a second 18 bit counter to control the force pulse.

5.6 Summary

Chapter 5 has detailed the analog error sources introduced in a generalized model of an 18 bit A/D loop for the seismic system. Total error depends on configuration; however, all the errors seem reasonable as long as a design is used which does not introduce large ripple components on the analog signal to be quantized. The binary force rebalance scheme is not recommended due to the prohibitive sample and hold design requirement.

CHAPTER 6

NOISE ANALYSIS OF ANALOG-TO-DIGITAL CONVERTER

6.1 Introduction

The loop used for this analysis is the analog-to-digital converter (A/D) (discussed in Chapter 5). It should be noted that noise estimates are highly dependent on the circuit configuration; therefore, this estimate is valid only for the loop topology selected, shown in Figure 6.1-1.

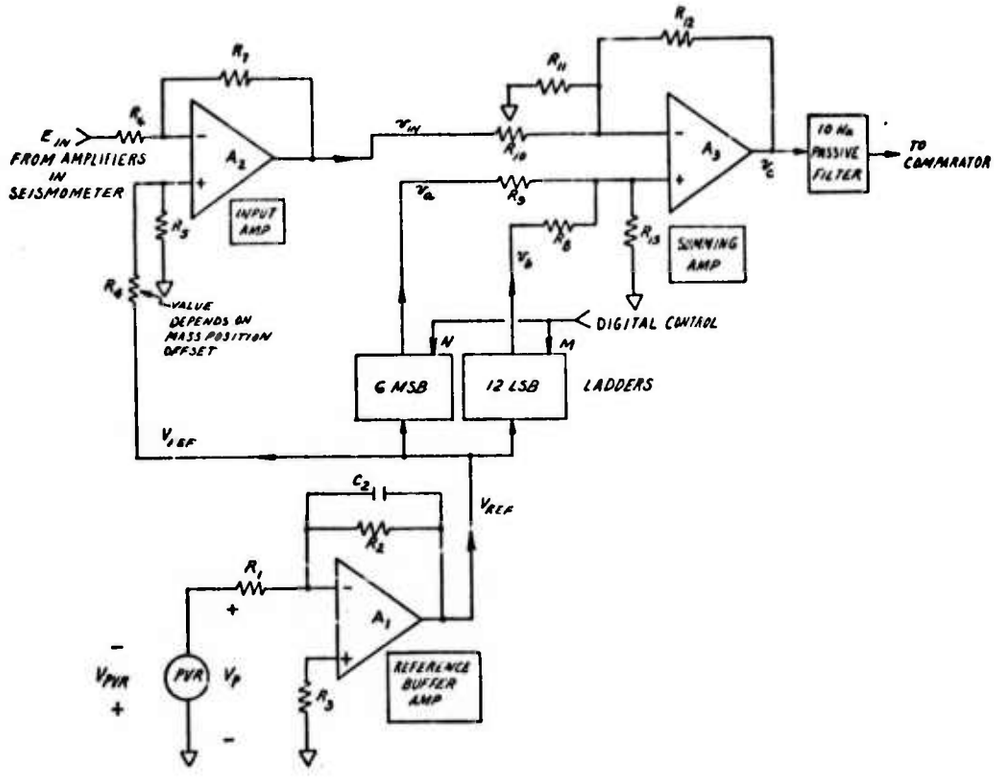

Fig. 6.1-1 Analog-to-Digital Converter

6.2 Definition of Noise Sources

6.2.1 Resistor Noise

Nyquist noise generated by the resistors is:

$$e_n = \sqrt{4kTBR}$$

or

$$e_n = 1.27 \times 10^{-10} \sqrt{BR} \quad \text{rms}$$

where B is the effective bandwidth and R is the resistance.

The highest bandwidth encountered in the design is 10 Hz and the maximum effective resistance is less than 10k Ω; therefore, the maximum expected noise from any resistor is:

$$e_n \cong 1.27 \times 10^{-10} \sqrt{10^5}$$

$$e_n \cong .04\mu V \text{ rms}$$

This value is negligible compared to other sources. Thus, the resistances in the circuit of Fig. 6.1-1 will be assumed noiseless.

6.2.2 Reference and Buffer (V_{REF})

Using the notation on Fig. 6.1-1 and the subscript n to indicate the noise component:

$$V_P = - (V_{PVR} + V_{PVR_n})$$

$$V_{REF} = - \frac{Z_2}{R_1} V_P - (1 + \frac{Z_2}{R_1}) A_{1n}$$

or:

$$V_{REF} = \frac{Z_2}{R_1} V_{PVR} + \frac{Z_2}{R_1} V_{PVR_n} - (1 + \frac{Z_2}{R_1}) A_{1n} \qquad (6\text{-}1)$$

where:

$$Z_2 = [\frac{R_2}{R_2 C_2 S + 1}]$$

6.2.3 Input Amplifier (v_{IN})

$$v_{IN} = \frac{R_5}{R_4} V_{REF} - \frac{R_7}{R_6} E_{IN} + (1 + \frac{R_7}{R_6}) A_{2n}$$

Substituting Eq. 6-1 into the above yields:

$$v_{IN} = \frac{R_5 Z_2}{R_1 R_4} V_{PVR} + \frac{R_5 Z_2}{R_1 R_4} V_{PVR_n} - \frac{R_5}{R_4} (1 + \frac{Z_2}{R_1}) A_{1n} - \frac{R_7}{R_6} E_{IN} + (1 + \frac{R_7}{R_6}) A_{2n} \quad (6\text{-}2)$$

6.2.4 Summing Amplifier (v_c)

$$v_a = \frac{N}{2^6} V_{REF}$$

$$v_b = \frac{M}{2^{12}} V_{REF}$$

$$v_c = \frac{R_{12}}{R_{10}} v_{IN} + \frac{R_{13}}{R_9} v_a + \frac{R_{13}}{R_8} v_b + (1 + \frac{R_{12}}{R_{10}}) A_{3n}$$

Reducing these equations yields:

$$v_c = \frac{R_{12}}{R_{10}} v_{IN} + [\frac{R_{13}}{R_9} \frac{N}{2^6} + \frac{R_{13}}{R_8} \frac{M}{2^{12}}] V_{REF} + (1 + \frac{R_{12}}{R_{10}}) A_{3n}$$

6.2.5 Total Noise Equation

Substituting Eqs. 6-1 and 6-2 into this expression yields:

$$\begin{aligned} v_c = & - \frac{R_{12} R_5 Z_2}{R_{10} R_1 R_4} V_{PVR} - \frac{R_{12} R_5 Z_2}{R_{10} R_1 R_4} V_{PVR_n} \\ & + \frac{R_{12} R_5}{R_{10} R_4} (1 + \frac{Z_2}{R_1}) A_{1n} + \frac{R_{12} R_7}{R_{10} R_6} E_{IN} \\ & - \frac{R_{12}}{R_{10}} (1 + \frac{R_7}{R_6}) A_{2n} + \frac{Z_2}{R_1} [\frac{R_{13}}{R_9} \frac{N}{2^6} + \frac{R_{13}}{R_8} \frac{M}{2^{12}}] V_{PVR} \\ & + \frac{Z_2}{R_1} [\frac{R_{13}}{R_9} \frac{N}{2^6} + \frac{R_{13}}{R_8} \frac{M}{2^{12}}] V_{PVR_n} \\ & - [1 + \frac{Z_2}{R_1}] [\frac{R_{13}}{R_9} \frac{N}{2^6} + \frac{R_{13}}{R_8} \frac{M}{2^{12}}] A_{1n} + (1 + \frac{R_{12}}{R_{10}}) A_{3n} \end{aligned} \quad (6\text{-}3)$$

As can be seen above, several of the noise terms are introduced in phase with each other and can be summed before the noise components are root sum squared. Grouping terms yields:

$$
\begin{aligned}
v_c = & \frac{R_{12}\,R_7}{R_{10}\,R_6}\,E_{IN} \\
& + \frac{Z_2}{R_1}\left[\left(\frac{R_{13}\,N}{R_9\;\;2^6} + \frac{R_{13}\,M}{R_8\;\;2^{12}}\right) - \frac{R_{12}\,R_5}{R_{10}\,R_4}\right] V_{PVR} \\
& + \frac{Z_2}{R_1}\left[\left(\frac{R_{13}\,N}{R_9\;\;2^6} + \frac{R_{13}\,M}{R_8\;\;2^{12}}\right) - \frac{R_{12}\,R_5}{R_{10}\,R_4}\right] V_{PVR_n} \\
& - \left(1 + \frac{Z_2}{R_1}\right)\left[\left(\frac{R_{13}\,N}{R_9\;\;2^6} + \frac{R_{13}\,M}{R_8\;\;2^{12}}\right) - \frac{R_{12}\,R_5}{R_{10}\,R_4}\right] A_{1n} \\
& - \frac{R_{12}}{R_{10}}\left(1 + \frac{R_7}{R_6}\right) A_{2n} \\
& + \left(1 + \frac{R_{12}}{R_{10}}\right) A_{3n}
\end{aligned}
\qquad (6\text{-}4)
$$

The first two terms in Eq. 6-4 are the signal terms, while the remaining terms are noise. We can now calculate the various output components of the noise due to the various noise sources.

6.3 Assumptions

The following assumptions are made before evaluating the noise defined by Equation 6-4:

1) Neglect resistor noise

2) Neglect ladder noise

3) Assume we place a 10 Hz filter on v_c that introduces no noise. Thus the comparator sees only the noise components below 10 Hz. The filter is placed at this point in the system because it is the most effective position to reduce the noise components introduced by the amplifiers. If filters are used on the feedback elements in amplifiers A2 and A3, only part of the noise introduced by A2 and A3 goes through the feedback filter. The remaining passes through with unity gain and no bandwidth

limiting. In addition, several of the noise sources would no longer cancel because of phase delays.

4) The filter on the PVR, Z_2, is assumed to rolloff at 10 Hz. This filter can be used in the feedback loop of A1 since phase delay here does not alter the cancellation of noise in later stages, though still reducing a part of the noise on V_{REF} above 10 Hz.

5) The resistor values and components determined in the proceeding sections will be used. These are by no means optimum.

6.4 Noise Computation

6.4.1 PVR Noise Component

Noise due to PVR =

$$\frac{Z_2}{R_1}\left[\left(\frac{R_{13}}{R_9}\frac{N}{2^6} + \frac{R_{13}}{R_8}\frac{M}{2^{12}}\right) - \frac{R_{12}}{R_{10}}\frac{R_5}{R_4}\right] V_{PVR_n}$$

Measured data on SIRU type PVR's gives values of about 1.8 μV rms for 400 Hz bandwidth. Over a 10 Hz bandwidth 1.0 μV rms would seem a reasonable estimate, since there is some 1/f noise present.

The worst case condition of noise due to the PVR occurs when full mass position offset is introduced ($R_4 = R_5$, and the digital control is supplying N = M = 0). For this case:

Noise due to PVR (worst case):

$$= 1.6 \times 10^{-6}$$

= 1.6 μV rms for 10 Hz bandwidth.

6.4.2 A1 Noise Component

Noise due to A1:

$$\left(1 + \frac{Z_2}{R_1}\right)\left[\left(\frac{R_{13}}{R_9}\frac{N}{2^6} + \frac{R_{13}}{R_8}\frac{M}{2^{12}}\right) - \frac{R_{12}}{R_{10}}\frac{R_5}{R_4}\right] A_{1n}$$

Worst case noise occurs under the same conditions as for the PVR, where N = M = 0 and $R_4 = R_5$.

6.4.3 HA 2904 noise is specified as dominantly voltage noise of 900 nV/$\sqrt{Hz}$ at 10 Hz, therefore:

$$A_{1n} = 2.84 \text{ } \mu V \text{ rms } (= A_{2n} = A_{3n})$$

Thus:

$$\begin{aligned} \text{Noise due to } A_1 &= (1 + 1.6) \times 1 \times 2.85 \text{ } \mu V \text{ rms} \\ &= 7.41 \text{ } \mu V \text{ rms} \\ &\quad \text{(for 10 Hz bandwidth)} \end{aligned}$$

6.4.4 A_2 Noise Component

$$\begin{aligned} \text{Noise due to } A_2 &= \frac{R_{12}}{R_{10}} \left(1 + \frac{R_7}{R_6}\right) A_{2n} \\ &= 1 \times 2 \times 2.85 \text{ } \mu V \\ &= 5.70 \text{ } \mu V \text{ rms} \\ &\quad \text{(for 10 Hz bandwidth)} \end{aligned}$$

6.4.5 A_3 Noise Component

$$\begin{aligned} \text{Noise due to } A_3 &= \left(1 + \frac{R_{12}}{R_{10}}\right) A_{3n} \\ &= 2 \times 2.85 \text{ } \mu V \\ &= 5.70 \text{ } \mu V \text{ rms} \\ &\quad \text{(for 10 Hz bandwidth)} \end{aligned}$$

6.4.6 Total Noise - Worst Case

The total noise at the output is the root sum square of the above sources:

$$\text{Total noise: } = \sqrt{1.6^2 + 7.41^2 + 5.70^2 + 5.70^2}$$

Total noise = 11.1 μV rms for 10 Hz bandwidth.

6.5 Summary

The derived value of 11.1 μV rms is the worst case. In a more realistic case only a small amount of offset will be used. For that case the noise level will be dependent on the digital control number driving the ladder. Figure 6.4-1 shows a graph of noise at the comparator versus the digital number, assuming various mass position offsets.

It should be noted that this noise estimate does not take into account the seismometer noise or the effect of the rate at which the A/D converter output is sampled. Both of these will affect the overall system noise.

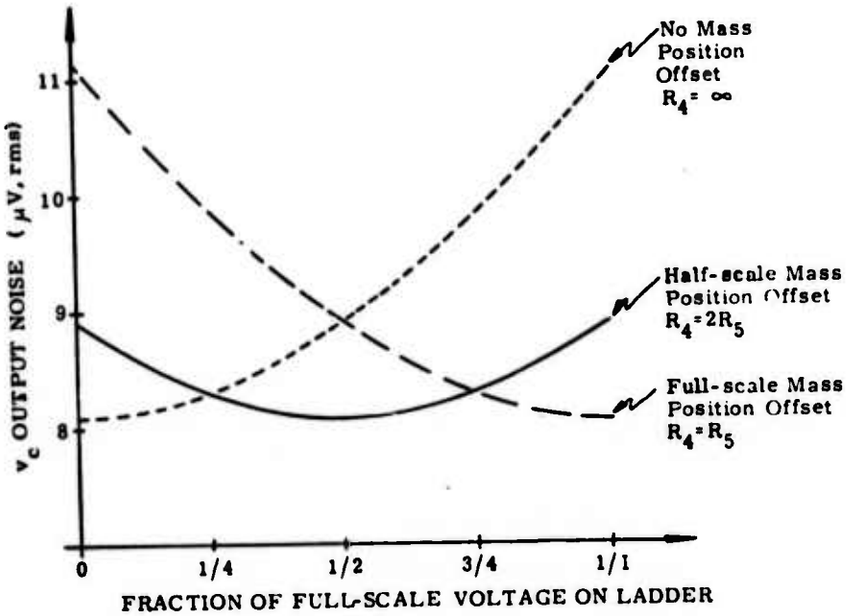

Fig. 6.4-1 Output Noise vs Fraction of Full Scale Ladder Voltage

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

The present study examined three separate approaches to implementing a feedback loop around the Geotech 36000 seismometer while providing a digitized output. The first approach, using a ternary pulse torque-to-balance loop was shown analytically to result in a generated noise signal (caused by the pulse torquing) which was input dependent and could not be removed effectively from the desired data signal.

The second approach, using a pulse width modulated loop, eliminated the problem encountered in the ternary implementation by constraining the pulse frequency to be constant and far enough removed from the desired data signal so as to permit a stable loop with good linearity and acceptably low noise. However, the pulse torquing gave rise to a large ripple signal riding on the output. This ripple, though tractable analytically, was of such magnitude that it produced insurmountable sampling problems in the electronics.

The third approach, using an analog loop with A/D conversion, proved to be the best alternative. Of the two possible implementations of such a loop, inboard or outboard of the feedback loop, the inboard implementation appears to be much superior.

The prime disadvantage of the external A/D converter is that its errors add directly to the other instrument errors and are not easily amenable to determination and compensation.

Using an A/D converter within the loop, as discussed in Chapter 3, retains the simplicity of the simple add-on external approach. But most important, almost all errors resulting from the A/D are reduced by the gain of the feedback loop, allowing for a more accurate and easily fabricated circuit.

The worst case noise resulting from the A/D conversion was found to be slightly higher than that generated within the seismometer (11 μV rms (0-10Hz) vs 4 μV rms (.02-1)). The overall system noise, with the inboard A/D,can be expected to be comparable to that with the present analog system.

For both inboard and outboard implementations, a relatively slow A/D can be used since the digitized signal is a "mirror" of the seismic signal and has the same low rate of change. There are no further sampling constraints at frequencies of interest, thereby reducing any aliasing problems. In short, from both analytical and electronics standpoints the use of an A/D converter inside the loop appears as an attractive, easily implemented, digital solution.

7.2 Recommendations

Based on the results of the foregoing study the following recommendations are presented:

1) An inboard A/D converter should be interfaced with a Geotech 36000 seismometer and the resultant performance evaluated at a "seismically quiet" site.

2) Comparison should be made of the seismometer performance for a totally analog configuration (as presently used) with that for the above described inboard A/D configuration.

3) An 18 bit A/D converter should be used. A larger range will require much greater cost and complexity in the electronics design. Such measures do not appear justified until more instrument performance data is available.

APPENDIX A

VOLTAGE REFERENCE AND SCALER ERRORS

V_{REF} TOLERANCE:

Resistors:	2 x .005%	=	.01%
PVR:	1%	=	1%
	Total	=	1.01%

V_{REF} OFFSET:

HA2904:

V_{off} x (1 + 1.6)	= 20 μV x 2.6	= 52 μV
Total I_{off} x 16000 x 1.6	= 2×10^{-10} x 16000 x 1.6	= 5.1μV
	Total	= 57.1μV

V_{REF} TC:

R_1R_2 tracking:	±1.5 ppm/°C x V_{PVR}	=	± 9.3 μV/°C
PVR:	±1 ppm/°C	=	± 10.0 μV/°C

HA2904:

ΔV_{off} x (1 + 1.6)	= .4 V/°C x 2.6	=	± 1.0 μV/°C
ΔI_{off} x 16000	= 3×10^{-12} x 16000	=	± 0.05μV/°C
	Total	≈	20 μV/°C

APPENDIX B

INPUT AMPLIFIER ERRORS

Signal Gain Tolerance:

2 x .005%	=	.01%

Offset Gain Tolerance:

2 x .005%	=	.01%
Total	=	.02%

Output Offset:

HA2904

V_{off} x (1 + 1) = 20 μV x 2	=	40 μV
I_{off} x 10^4 = 2 x 10^{-10} x 10^4	=	2 μV
Total	=	42 μV

Signal Gain TC:

R_1R_2 1.5 ppm/°C tracking	=	±1.5 ppm/°C

Offset Gain TC:

R_3R_4 1.5 ppm/°C tracking	=	±1.5 ppm/°C

Amplifier Offset TC:

HA2904

ΔV_{off} x (1 + 1) = .4 μV/°C x 2	=	± .8 μV/°C
ΔI_{off} x R_4 = 3 x 10^{-12}A/°C x 10^4	=	± .03 μV/°C
Total	=	± .8 μV/°C

APPENDIX C

SUMMING AMPLIFIER ERRORS

Signal Gain Tolerance:

3 x .005%	=	.015%

Ladder Gain Tolerance:

3 x .005%	=	.015%

Output Offset (HA2904):

V_{off} x (1 + 1) = 20 μV x 2	=	40 μV
I_{off} x 10k = 2 x 10^{-10} x 10^{4}	=	2 μV
Total	=	42 μV

Signal Gain T.C.:

R_0, R_{20}, R_{10}
TC Tracking: 1.5 ppm/°C

Ladder Gain TC:

R_a, R_b, R_c
TC Tracking: 1.5 ppm/°C

Amp Offset TC (HA2904):

ΔV_{off} x (1 + 1) = .4 μV/°C x 2	=	±.8 μV/°C
ΔI_{off} x 10^{4} = 3 x 10^{-12} A/°C x $10^{4}\Omega$	=	± .03 μV/°C
Total	=	±.8 μV/°C

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